Prerana Educational and Social Trust®
PES Institute of Technology and Management
NH-206,Sagar Road,Shivamogga-577204
Department of Electronics and Communication Engineering

DIGITAL SYSTEM DESIGN USING VERILOG

Subject code; 15EC663

Course File

Academic Year-2018-19

Prepared by

Mr. Kunjan D. Shinde

Asst. Professor, Dept. of E&CE, PESITM

PES Institute of Technology and Management

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

Course File Check List

Sl. No	Particulars	
1.	VTU COE	
2.	College COE	
3.	Dept. COE	
4.	Syllabus	
5.	CO – PO mapping	
6.	Time Table (Class)	
7.	Time Table (Individual)	
8.	Student List	
9.	IA question papers with scheme	
10.	List of IA marks and final IA marks	
11.	IA analysis	Poor performers
		Top performers
		Action Taken Report
12.	University IA marks	
13.	Attainment	
14.	Question Bank	
15.	Lesson plan (detailed)	
16.	VTU question papers	

Revised Academic Calendar of VTU, Belagavi for EVEN Semester of 2018-2019 (Feb 2019 – July 2019)

	II Sem B. E. / B. Tech. / B. Arch	IV & VI Sem B. E. /B. Tech. IV, VI,VIII Sem B. Arch.	VIII Sem B.E / B.Tech & X Sem B. Arch	IV Sem MCA	VI Sem MCA	IV Sem MBA	IV Sem M. Tech.	IV Sem M. Arch.	II Sem M. Tech.	II Sem MCA	II Sem MBA	II Sem M. Arch.
Commencement of EVEN Semester	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Last Working day of EVEN Semester	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Practical Examination	19.06.2019 To 29.06.2019	27.05.2019 To 07.06.2019	-	21.05.2019 To 25.05.2019	-	-	-	-	24.06.2019 To 29.06.2019	24.06.2019 To 29.06.2019		-
Theory Examinations	01.07.2019 To 16.07.2019	10.06.2019 To 16.07.2019	27.05.2019 To 07.06.2019	27.05.2019 To 15.06.2019	-	03.06.2019 To 28.06.2019	27.05.2019 To 31.05.2019	-	01.07.2019 To 12.07.2019	01.07.2019 To 12.07.2019	20.06.2019 To 04.07.2019	20.06.2019 To 04.07.2019
Viva Voce		-	11.06.2019 To 17.06.2019	-		-	-	-	-	-	-	-
Summer Project / Professional training							[illegible]					
Commencement of ODD Semester	22.07.2019	22.07.2019	-	22.07.2019	-		-	-	26.08.2019	22.07.2019	08.08.2019	22.07.2019

NOTE

1. College Time Table shall be arranged for five and a half week days and planned to accommodate EDUSAT transmission slots, the schedule of which will be notified separately.
2. The faculty/staff shall be available to undertake any work assigned by the university.
3. If any of the above date is declared to be a holiday then the corresponding event will come into effect on the next working day.
4. Notification regarding Calendar of Events relating to the conduct of University Examination will be issued by the Registrar (Evaluation) from time to time

Professor & Head
Dept. of Electronics & Comm Engg
[illegible]

REGISTRAR

PES INSTITUTE OF TECNOLOGY AND MANAGEMENT, Shimoga

Calendar of Events During Second semester -2018-19 (Tentative)

Month			Dates				Days/Festivals	Academic activities
FEBRUARY	FRI		1	8	15	22		
	SATUR		2	9	16	23		04/02/2019 Reopening - II Sem
	SUN		3	10	17	24		Placement/ Soft-skill Training, 20th Feb to 23rd Feb, 4 days for II Sem .
	MON		4	11	18	25		
	TUE		5	12	19	26		
	WED		6	13	20	27		
	THUR		7	14	21	28		
	FRI	1	8	15	22			
	SATUR	2	9	16	23			
	SUN	3	10	17	24			
MARCH	MON		4	11	18	25	04th Maha Shivarathri	2nd Ethnic Day
	TUE		5	12	19	26		13th Dispatch of First IA Report
	WED		6	13	20	27		
	THUR		7	14	21	28		
	FRI	1	8	15	22	29		
	SATUR	2	9	16	23	30		
	SUN	3	10	17	24	31		
APRIL	MON		1	8	15	22	29 Sri Krishnamana Yugadi	11, 12, 13 - First - I A for II Semester
	TUE		2	9	16	23	30 14th Mahaveer Jayanthi	40% of the Syllabus for First IA
	WED		3	10	17	24	19th Good Friday	Dispatch of Second IA Report
	THUR		4	11	18	25	20th working day compensatory for 18th.	26th Sports Day
	FRI		5	12	19	26	21st to followed on 21st.	27th College Day
	SATUR		6	13	20	27	22nd working day compensatory for 20th.	
	SUN		7	14	21	28		
	MON		8	15	22	29	01st May Day	15, 16, 17 - Second IA for II Semester
MAY	TUE		9	16	23	30	07th Basava Jayanthi	35% of the Syllabus for Second IA
	WED	1	10	17	24	31		22nd Dispatch of Second IA report
	THUR	2	11	18	25			
	FRI	3	12	19	26	1		
	SATUR	4	13	20	27	2		
	SUN	5	14	21	28	3		
	MON	6	15	22	29	4		
	TUE		16	23	30	5	18 Ramzan	13, 14, 15-Third IA for II Semester
JUNE	WED		17	24		6		Last 25% of the Syllabus for Third IA
	THUR		18	25		7		
	FRI		19	26		8		
	SATUR		20	27		9		
	SUN		21	28		10		
	MON		22	29		11		
	TUE		23	30		12		
	WED		24	31		13		
	THUR		25			14		
	FRI		26			15		
	SATUR		27			16		
	SUN		28			17		

Director

Principal

Dept. of Electronics & Comm Engg
PES Institute of Technology & Management
Shivamogga-577204

PES INSTITUTE OF TECHNOLOGY & MANAGEMENT, SHIVAMOGGA
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CALENDER OF EVENTS OF EVEN SEMESTER-2019

WEEK	MONTHS	SUNDAY	MONDAY	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY	SATURDAY	WORKING DAYS	REMARKS
1	JAN/FEB	27	28	29	30	31	1	2	6	Commencement of Even Semester
2	FEB	3	4	5	6	7	8	9	6	
3	FEB	10	11	12	13	14	15	16	6	
4	FEB	17	18	19	20	21	22	23	6	
5	FEB/MAR	24	25	26	27	28	1	2	6	
6	MAR	3	4	5	6	First IA Test			5	Mahashivarathri
7	MAR	10	11	12		14	15	16	6	
8	MAR	17	18	19	20	21	22	23	6	
9	MAR	24	25	26	27	28		30	6	
10	MAR/APR	31	1	2	3	4	5	6	5	Chandramana Yugadi
11	APR	7	8	9	10	Second IA Test			6	
12	APR	14	15	16	17	18	19	20	2	Mahaveer Jayanthi Good Friday
13	APR	21	22	23	24.	25	26	27	6	
14	APR/MAY	28	29	30	1	2	3	4	5	May Day
15	MAY	5	6	7	8	9	10	11	5	Basava Jayanthi
16	MAY	12	13	14	Third IA Test			18	6	
17	MAY	19	20	21	22	23	24	25	6	
								No of Working Days	94	

Last Working Day of even sem	
Practical Exams // Project Viva Voce	
Theory Exams	
Commencement of Even sem	

General Holiday

Professor & Head
Dept. of Electronics & Comm Engg
PESITM, Shivamogga-577204

DIGITAL SYSTEM DESIGN USING VERILOG
B.E., VI Semester (Open Elective)
[As per Choice Based Credit System (CBCS) scheme]

Subject Code:	15EC663	IA Marks: 20
Number of Lecture Hours/Week:	**03**	Exam Marks: 80
Total Number of Lecture Hours:	40 (08 Hrs per module)	Exam Hours: 03

CREDITS – 03

Course objectives: This course will enable students to:
• Understand the concepts of Verilog Language. • Design the digital systems as an activity in a larger systems design context. • Study the design and operation of semiconductor memories frequently used in application specific digital system. • Inspect how effectively IC's are embedded in package and assembled in PCB's for different application. • Design and diagnosis of processors and I/O controllers used in embedded systems.

Module 1	RBT Level
Introduction and Methodology: Digital Systems and Embedded Systems, Real-World Circuits, Models, Design Methodology (1.1, 1.3 to 1.5 of Text). **Combinational Basics:** Combinational Components and Circuits, Verification of Combinational Circuits.(2.3 and 2.4 of Text) **Sequential Basics**: Sequential Datapaths and Control Clocked Synchronous Timing Methodology (4.3 up to 4.3.1,4.4 up to 4.4.1 of Text).	L1, L2, L3
Module -2	
Memories: Concepts, Memory Types, Error Detection and Correction (Chap 5 of Text)	L1, L2, L3
Module -3	
Implementation Fabrics: Integrated Circuits, Programmable Logic Devices, Packaging and Circuit boards, Interconnection and Signal integrity (Chap 6 of Text).	L1, L2, L3
Module -4	
I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software (Chap 8 of Text).	L1, L2, L3
Module -5	
Design Methodology: Design flow, Design optimization, Design for test, Nontechnical Issues (Chap 10 of Text).	L1, L2, L3, L4

Course outcomes: After studying this course, students will be able to:
• Construct the combinational circuits, using discrete gates and programmable logic devices. • Describe Verilog model for sequential circuits and test pattern generation. • Design a semiconductor memory for specific chip design. • Design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores. • Synthesize different types of processor and I/O controllers that are used in embedded system.

Question paper pattern:
• The question paper will have ten questions. • Each full Question consisting of 16 marks. There will be 2 full questions (with a maximum of Three sub questions from each module. • Each full question will have sub questions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module.

Text Book: Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elesvier, 2010.

Mr. Kunjan D. Shinde
Assistant Professor, Dept. of E&CE, PESITM, Shivamogga.

STUDENT LIST 6TH A

Sl. No.	Name	USN
1	PALLAVI	4PM14EC048
2	ANGEL PRIYA M	4PM15EC006
3	ANUSHREE KAMATH	4PM15EC007
4	GANESH P D M	4PM15EC029
5	MADHU S BHAT	4PM15EC041
6	MEGHARAJACHARI	4PM15EC045
7	NEHA P	4PM15EC051
8	ABISHEK J M	4PM16EC001
9	AISHWARYA CH	4PM16EC002
10	AISHWARYA S K	4PM16EC004
11	AKSHAY KUMAR M	4PM16EC005
12	ANUSHA B G	4PM16EC007
13	ANUSHA N S	4PM16EC008
14	ARPITHA L	4PM16EC010
15	ARUN KUMAR N M	4PM16EC011
16	ASHA G M	4PM16EC012
17	BHARATH M	4PM16EC013
18	CHAITHRA C	4PM16EC014
19	CHAITHRA K C	4PM16EC015
20	DEEKSHITH B	4PM16EC017
21	DEEPA HONDAD	4PM16EC018
22	DIXITHA C SHET	4PM16EC020
23	DUNDUBI R	4PM16EC021
24	GANAVI C G	4PM16EC022
25	GANESHA N	4PM16EC023
26	GIRIRAJA SWAMY NP	4PM16EC024
27	GURUPRASAD D	4PM16EC025
28	HALASWAMY S R	4PM16EC026
29	HARSHA M S	4PM16EC027
30	HARSHITHA B	4PM16EC028
31	HARSHITHA M K	4PM16EC029
32	HARSHITHA S	4PM16EC030
33	K S NAGASHREE	4PM16EC032
34	KAVYA G C	4PM16EC033
35	KAVYA R	4PM16EC034
36	KEERTHANA R	4PM16EC035
37	LAVANYA A	4PM16EC036
38	LIKITHA R	4PM16EC037
39	M MONISHA	4PM16EC038
40	MADHUSHREE S S	4PM16EC039
41	MANJANAIK S B	4PM16EC040
42	NAGASHREE V S	4PM16EC041
43	NEHA D G	4PM16EC042
44	NEHASHRI S	4PM16EC043
45	NIDA KHANUM	4PM16EC044
46	NIHAR K K	4PM16EC045
47	NIHARIKA B H	4PM16EC046
48	NIKHIL JOSEPH	4PM16EC047
49	NITHIN S M	4PM16EC048
50	PADMASHREE A	4PM16EC049
51	PALLAVI M P	4PM16EC050
52	NITISH BHARDWAJ	4PM16EC103
53	CHETANA B C	4PM16EC403
54	MARUTHI T L	4PM16EC412
55	ABHISHEK GOWDA	4PM17EC401
56	BHARATHKUMAR H	4PM17EC403
57	KAVYA B	4PM17EC405
58	LOKESH C	4PM17EC408
59	PRAMODKUMAR S	4PM17EC412

Professor & Head
Dept. of Electronics & Comm Engg
PESITM, Shivamogga-577204

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

INDIVIDUAL TIME TABLE

Faculty Name:Mr. Kunjan D. Shinde

Designation: Assistant Professor

DAY/TIME	08.00 - 09.00	09.00 - 10.00	10.00 - 10.30	10.30 - 11.30	11.30 - 12.30	12.30 - 01.30	01.30 - 02.30	02.30 - 03.30	03.30 - 04.30	04.30 - 05.00
Monday	NS			DSDV						
Tuesday				DSDV	NS		EMDC LAB – A3			
Wednesday	EMDC LAB – A2				DSDV					
Thursday										
Friday	NS	DSDV								
Saturday		NS								

WORKLOAD DISTRIBUTION

Sl. No.	Sem	Subject Code	Subject / Lab / other if any	Workload		Total Units	Additional Responsibility
				In hours	In Units		
1	6th A	15EC663	Digital System Design Using Verilog	4	8	27	ISO Coordinator, Forum/Technical Talk/Workshop, NSS Coordinator
2	8th	10EC832	Network Security	4	8		
3	6th A	15ECL67	Embedded Controller Lab	3	3		
4	6th B	15ECL67	Embedded Controller Lab	6	6		
5	8th		Project Work + Seminar	-	2		

Signature of the HOD
Dr. Chandrappa D N

Program outcomes (POs)

Engineering Graduates will be able to:

PO1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

ECE graduates will be able to:

PSO1. Analyze and design analog & digital circuits or systems for a given specification and function.

PSO2. Implement functional blocks of hardware-software co-designs for signal processing and communication applications.

Digital System Design using Verilog

Subject Code: 15EC663

Prerequisites:

Basic knowledge of Digital Electronics,Verilog HDL.

Course Outcomes:

CO1	Construct the combinational circuits, using discrete gates and programmable logic devices.
CO2	Describe Verilog model for sequential circuits and test pattern generation.
CO3	Design a semiconductor memory for specific chip design.
CO4	Design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores.
CO5	Synthesize different types of processor and I/O controllers that are used in embedded system.

Course Outcome to Program Outcome Mapping:

1: LOW 2: MEDIUM 3: HIGH

PO	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2
CO1	3	2	1	2									2	1
CO2	2	2	3	2									3	2
CO3	2	2	3	2									3	2
CO4	2	2	3	3									3	2
CO5	2	2	2	2									2	1
Planed	2.2	2	2.4	2.2									2.6	1.6
Attained														

Questionnaires for CO

Can you construct the combinational circuits, using discrete gates and programmable logic devices.
Are you able to describe Verilog model for sequential circuits and test pattern generation.
Are you able to design a semiconductor memory for specific chip design.
Are you able to design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores.
Can you synthesize different types of processor and I/O controllers that are used in embedded system.

Lesson Plan

Department of Electronics and Communication Engineering

Semester: VI

Subject Name:	Digital System Design Using Verilog	*Subject Code*:	15EC663
Hours / week: L-T-P	03-00-00	*Total Hours:*	40
Exam Marks / Credits	80/3	*IA Marks*:	20
Lesson Plan Author:	Mr. Kunjan D Shinde Mr.Vishwanath Muddi	*Duration of Exam*:	03 Hrs
Checked By:	Dr. Chandrappa D N	*Date*:	29/01/2019

A. **Course Prerequisites:** Students should have the fundamental knowledge of

Description	Course Name	Code	Semester
Basics of Digital electronics	Digital Electronics	15EC33	III
Basics of Verilog coding	Verilog HDL	15EC53	V

C. Course learning objectives (CLOs):

CLO1	Understand the concepts of Verilog Language
CLO2	Design the digital systems as an activity in a larger systems design context
CLO3	Study the design and operation of semiconductor memories frequently used in application specific digital system
CLO4	Inspect how effectively IC's are embedded in package and assembled in PCB's for different application
CLO5	Design and diagnosis of processors and I/O controllers used in embedded systems.

D. Modes of content delivery:

The following are the various content delivery methods considered in the program:

- M1: Lecture delivery with discussion (blackboard teaching)
- M2: Tutorial (problem solving / discussions classes)
- M3: Presentations (PPT)
- M4: Experimental demonstration
- M5: Remedial Classes (Extra Classes)
- M6: Animations video files

D. Course Syllabus:

Part –A

Module -1 **Introduction and Methodology:** Digital Systems and Embedded Systems, Real-World Circuits, Models, Design Methodology (1.1, 1.3 to 1.5 of Text). **Combinational Basics**: Combinational Components and Circuits, Verification of Combinational Circuits.(2.3 and 2.4 of Text) **Sequential Basics:** Sequential Datapaths and Control Clocked Synchronous Timing Methodology (4.3 up to 4.3.1,4.4 up to 4.4.1 of Text).	**08 hrs**
Module -2 **Memories**: Concepts, Memory Types, Error Detection and Correction (Chap 5 of Text).	**08hrs**
Module -3 **Implementation Fabrics:** Integrated Circuits, Programmable Logic Devices, Packaging and Circuit boards, Interconnection and Signal integrity (Chap 6 of Text).	**08hrs**
Module -4 **I/O interfacing:** I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software (Chap 8 of Text).	**08hrs**
Module -5 **Design Methodology:** Design flow, Design optimization, Design for test, Nontechnical Issues (Chap 10 of Text).	**08hrs**

Scheme of Continuous Internal Evaluation (CIE): As per VTU norms

Question paper pattern:

Assessment	Marks
Internal Assessment Exam 1	20
Internal Assessment Exam 2	20
Improvement- Internal Assessment Exam 3	20
Assignments	---
Total	**20**

Text Books:

1. Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elesvier, 2010.

E: Course Outcome (COs):

After studying this course, students will be able to:

CO1	Construct the combinational circuits, using discrete gates and programmable logic devices.
CO2	Describe Verilog model for sequential circuits and test pattern generation.
CO3	Design a semiconductor memory for specific chip design.
CO4	Design embedded systems using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores.
CO5	Synthesize different types of processor and I/O controllers that are used in embedded system.

F: Programme Outcomes addressed to the course (POs)

G: Gaps in the syllabus to meet Industry requirement:

1.
2.

H: Topics Beyond syllabus / Advanced Topics:

1.
2.

I: Assessment Methodologies:

SNO	Description	Type
1	Student Assignment	Direct
2	Internal Assessment test	Direct
3	University Examination	Direct
4	Student feedback	Indirect

Topic Level Plan

Topic Name : Introduction and Methodology, Combinational basics, Sequential basics	**Module No : 01**
	Duration: 8 Hrs

Topic Level Objectives(TLOs) :

1. To understand the basic ideas of digital abstraction and digital circuit elements.
2. To focus on combinational logic circuits starting with Boolean algebra.
3. To describe sequential circuit elements for storing information and for counting events.

Topic Learning Outcomes:

At the end of the topic, the students will be able to,

1. **Explain** the benefits of digital approach..
2. **Design** various combinational logic circuits.
3. **Design** data path and control section in the digital circuits.

Review Questions:

1. What is meant by the term fanout?.
2. What are the two sources of power consumption in a digital component?
3. What are the TTL output voltage levels, input threshold voltages and noise margins?
4. What is meant by the terms setup time, hold time and clock-to-output time of a fl ip-flop?.
5. For a decoder with inputs (a2, a1, a0), write the Boolean equation for the output corresponding to the code word 100.

Critical Questions:

1 Identify two approaches to functional verification.

2 What information is specified for each port in a Verilog module?

3 If verification fails during some stage of a design methodology, what action is taken?

4 Develop a Verilog model for a 4-to-1 multiplexer.

5 How does a priority encoder solve the problem of multiple inputs being 1 at the same time?

Challenging Questions:

1 Develop a Verilog model for a 7-segment decoder.

2 Design an encoder for use in a domestic burglar alarm that has sensors for each of eight zones. Each sensor signal is 1 when an intrusion is detected in that zone, and 0 otherwise. The encoder has three bits of output, encoding the zone as follows: Zone 1: 000 Zone 2: 001 Zone 3: 010 Zone 4: 011 Zone 5: 100 Zone 6: 101 Zone 7: 110 Zone 8: 111

3 How can we construct a 2-to-1 multiplexer for 5-bit encoded data inputs?

Topic Name : Memories:	Module No : 02 Duration: 08 Hrs

Topic Level Objectives(TLOs) :

1. To understand the use of memories.
2. To understand the features of semiconductor memory.
3. To understand the techniques for dealing with errors in the stored data.

Topic Learning Outcomes:

At the end of the topic, the students will be able to

1. Explain the use of memories and various types of memories.
2. Explain the particular features of each type memories, including SRAM, DRAM, ROM and flash memories.
3. Solve the problems related to memory error detection and correction.

Review Questions

1. What are the three states of a tristate driver?
2. How do memory components with tristate data outputs simplify construction of large memories?
3. What is the difference between RAM and ROM?
4. What is the difference between static and dynamic RAM?
5. What benefit does a multiport memory have over a single-port memory with multiplexed address and data connections?

Challenging Questions:

1. How does a FIFO facilitate communication of data between clock domains?
2. How can we work out what will happen if we perform concurrent writes to a given location in a synchronous dual-port memory?
3. Using a Hamming code, how many check bits are required for single error correction and double-error detection for 4-bit data words?
4. What corrective action can we take when a parity error is detected?
5. Compute the 12-bit ECC word corresponding to the 8-bit data word 01100001.

Topic Level Plan

Topic Name : Implementation Fabrics	**Module No : 03**
	Duration: 08 Hrs

Topic Level Objectives(TLOs) :

1. To know about different range of integrated circuits used to implement Digital circuits
2. To understand Programmable logic Devices
3. To understand the important characteristics of integrated circuits and printed circuit boards that give rise to constraints on Digital circuit designs.

Topic Learning Outcomes:

At the end of the topic, the students will be able to

1. **Distinguish:** FPGA, CPLDs and ASIC used for implementing Digital circuits.
2. **Explain:** The purposes of logic blocks and I/O blocks in an FPGA
3. **Explain:** The factors affecting packaging and signal integrity

Review Questions:

1. What is photolithography in IC manufacture?
2. How do IC area and defect density on a wafer affect IC cost?
3. What do the terms *ASIC* and *ASSP* stand for?
4. How does a programmable logic device differ from a fixed-function component?
5. What is a fuse map?

Critical Questions:

1. Use the following components to design a 4-digit decimal counter with a 7-segment LED display: two 74LS390 dual decade counters, four 74LS47 BCD to 7-segment decoders, four 7-segment displays, plus any additional gates required.
2. Derive an expression for the short –circuit trans conductance G_m of the MOS cascade amplifier.
3. If an FPGA uses volatile SRAM cells to store configuration information, how is the configuration information stored and supplied to the FPGA?
4. For a 2.5V low-voltage differential signaling (LVDS) output, the nominal VOL and VOH voltages are 1.075V and 1.425V, respectively. What differential voltage swing is seen at the receiver?

Challenging Questions:

1. Design a priority encoder that has 16 inputs, I[0:15]; a four-bit encoded output, Z[3:0]; and a valid output that is 1 when any input is 1. Input I[0] has the highest priority, and I[15] the lowest priority. The design is to be implemented in a GAL22V10 component.
2. Use the following components to design a 4-digit decimal counter with a 7-segment LED display: two 74LS390 dual decade counters, four 74LS47 BCD to 7-segment decoders, four 7-segment displays, plus any additional gates required.

Topic Level Plan

Topic Name : I/O Interfacing	**Module No : 04**
	Duration: 08 Hrs

Topic Level Objectives(TLOs) :

1. To understand the operation of Different I/O Devices
2. To understand Operation I/O Controllers.
3. To Design a verilog model for different I/O devices.

Topic Learning Outcomes:

At the end of the topic, the students will be able to

1. **Define:** Sensors and Actuators
2. **Explain:** Working of communication protocols like UART, I2C and SPI.
3. **Design:** Verilog models for I/O interfacing by using various communication protocols.

Review Questions:

1. What is a sensor? What is an actuator?
2. Why would a digital system require a digital-to-analog converter?
3. How many comparators are required in a flash ADC with a resolution of 8 bits?
4. What is the difference between a solenoid and a relay?
5. What is the purpose of an input register in an I/O controller? What is the purpose of an output register?

Critical Questions:

1. Write a Verilog statement to model a tri-state driver for an output net d_out. The driver is controlled by a net d_en, and when enabled, drives the value of an input d_in onto the output net.
2. In a multiplexed bus system, why might it be desirable to subdivide the multiplexers and distribute them around the chip?

Challenging Questions:

1. Show how a 64-bit data word can be transmitted serially between two parts of a system. Assume that the transmitter and the receiver are both within the same clock domain, and that the signal start is set to 1 on a clock cycle in which data is ready to be transmitted.
2. Design an interface to connect an embedded Gumnut core to a remote temperature sensor. The temperature sensor is an Analog Devices AD7414 with an I2C connection and an alert output that can be connected to a warning indicator.

Topic Level Plan

Topic Name : Design Methodology	**Module No : 05**
	Duration: 08 Hrs

Topic Level Objectives(TLOs) :

1. To understand Digital design flow in detail
2. To understand Behavioral model of a component.
3. To understand Design for test models

Topic Learning Outcomes:

At the end of the topic, the students will be able to

1. **Explain**: the concept term architecture exploration
2. **Discuss:** the importance Design for test models.
3. **Distinguish**: between logical partitions and physical partitions.
4. **Identify**: some advantages and disadvantages of formal verification over simulation-based testing.
5. **Explain:** the purpose of floor planning, placement, and routing.

Review Questions:

1. What is meant by the term architecture exploration?
2. What is the distinction between logical partitions and physical partitions of a system?
3. What are the benefits of reusing an IP block to implement a component?
4. Briefly describe the purpose of floor planning, placement, and routing.
5. Why should clock gating not be implemented in RTL model code? How is it better implemented?

Critical Questions:

1. Describe the difference between code coverage and functional coverage. Which is more important for ensuring correctness of a design?
2. How does IDDQ testing detect transistor stuck-on faults?
3. What purposes do LFSRs and MISRs have in signature-based BIST?
4. Identify some of the main stages in a product's life cycle.

Challenging Questions:

1. Identify a means of improving system performance that we might consider in the architecture exploration stage. What trade-offs arise from improving performance?
2. Synthesize and implement the Sobel accelerator design targeting a Xilinx XC3S200-5 Spartan-3 FPGA with a clock frequency of 100MHz (that is, a clock period of 10ns).
3. Design the control section to sequence computation of the derivative image.

Activity Schedule

Activities	Announcement Date	Submission Date	Evaluation Date	HOD's Remarks
Assignment				
Quiz				
Course Seminar				
Course Project				
Subject Proficiency Test/Skill Test				
Note: Faculty shall conduct minimum of two of the five activities stated above				

Course Articulation Matrix

Course Learning Outcomes	Activities that meet the outcomes	Program Outcomes											
		a	b	c	d	e	f	g	h	i	j	k	l
CLO-1	Assignment, quiz	H	M	L	M								
CLO-2	Assignment, quiz	M	M	H	M								
CLO-3	Assignment, quiz	M	M	H	M								
CLO-4	Assignment, quiz	M	M	M	H								
CLO-5	Assignment, quiz	M	M	M	M								

L: Low M: Medium H: High

Level of achievement of programme outcome .

PO	Description
A	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering
B	**Problem analysis:** Identify, formulate, research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
C	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety, and cultural, societal, and environmental considerations.
D	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
E	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modeling to complex engineering activities, with an understanding of the limitations.
F	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal, and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

G	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
H	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice
I	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
J	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with the society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
K	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
L	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Checklist:

Sl. No.	Items		HOD's Remarks
1	Assignments	☐	
2	Quiz Questions	☐	
3	I.A. Q Paper /Evaln. Schemes	☐	
4	Syllabus Copy	☐	
5	PPTs/OHP sheets	☐	
6	Lesson Plan	☐	
7	VTU Question Papers	☐	
8	Attendance book	☐	
10	GATE/PGCET Question papers	☐	
11	Course Project Definitions	☐	
12	Tutorials	☐	

Faculty signature & name with date:
Mr. Kunjan D. Shinde 15/12/19
Mr. Vishwanath Muddi.

Remarks by HOD:

HOD's Signature & name with date

Lesson Schedule

Department: Electronics and Communication Engg. **Name of Faculty** : Mr. Kunjan D. Shinde
Title of the subject: Digital System Design Using Verilog **Sub Code:** 15EC663 **No. of hours** : 40

Lecture No.	Unit / Module No.	Topics to be covered	Date Scheduled	Date of Delivery	Specify mode of Content delivery (Blackboard, PPT, Video, others)	Remarks
1	1	Digital Systems and Embedded Systems.	04/02/2019 05/02/2019	05/2/19	Blackboard	Completed
2	1	Real-World Circuits	06/02/2019 08/02/2019	08/2/19	Blackboard	Completed
3	1	Models. Design Methodology	11/02/2019	11/2/19	Blackboard	Completed
4	1	Combinational Components and Circuits	12/02/2019	13/2/19	Blackboard	Completed
5	1	Verification of Combinational Circuits	13/02/2019 15/02/2019	19/2/19	Blackboard	Completed
6	1	Sequential Data paths	19/02/2019	22/2/19	Blackboard	Completed
7	1	Control Clocked Synchronous Timing Methodology	18/02/2019 19/02/2019	25/2/19	Blackboard	Completed
8	1	Control Clocked Synchronous Timing Methodology	20/02/2019	26/2/19	Blackboard /PPT	Completed
9	2	**Memories**: Concepts	22/02/2019	27/2/19	Blackboard	Completed
10	2	Memory Types	25/02/2019	01/3/19	Blackboard	Completed

11	2	Memory Types	26/02/2019	05/03/19	Blackboard	Completed
12	2	Error Detection and Correction	27/02/2019	08/03/19	Blackboard	Completed
13	2	Error Detection and Correction	01/03/2019	12/03/19	Blackboard	Completed
14	2	Error Detection and Correction	05/03/2019	13/03/19.	Blackboard	Completed
15	2	Error Detection and Correction	11/03/2019	15/03/19	Blackboard	Completed
16	2	Error Detection and Correction	12/03/2019	18/03/19.	PPT,Video	Completed
17	3	**Implementation Fabrics**: Integrated Circuits	13/03/2019		Blackboard	Completed
18	3	Programmable Logic Devices	15/03/2019 18/03/2019	19/3/19	Blackboard	Completed
19	3	Programmable Logic Devices	19/03/2019	20/3/19	Blackboard	Completed
20	3	Packaging and Circuit boards	20/03/2019	25/3/19	Blackboard	Completed
21	3	Packaging and Circuit boards	22/03/2019	26/3/19	Blackboard	Completed
22	3	Interconnection and Signal integrity	25/03/2019	27/3/19	Blackboard	Completed
23	3	Interconnection and Signal integrity	26/03/2019	29/3/19	Blackboard	Completed
24	3	Interconnection and Signal integrity	27/03/2019 29/03/2019	30/3/19	Blackboard /PPT	Completed
25	4	**I/O interfacing:** I/O devices	01/04/2019	2/4/19	Blackboard	Completed
26	4	I/O controllers	02/04/2019	5/4/19	Blackboard	Completed
27	4	Parallel Buses	03/04/2019	8/4/19	Blackboard	Completed
28	4	Parallel Buses	05/04/2019	9/4/19	Blackboard	Completed
29	4	Serial Transmission	08/04/2019	10/4/19	Blackboard	Completed
30	4	Serial Transmission	09/04/2019	15/4/19	Blackboard	Completed.

31	4	I/O software	10/04/2019	16/4/19	Blackboard	Completed
32	4	I/O software	12/04/2019 15/04/2019	16/4/19	Blackboard	Completed
33	5	Design Methodology: Design flow	21/04/2019 22/04/2019	24/4/19	Blackboard	Completed
34	5	Design flow	23/04/2019	3/5/19	Blackboard	Completed
35	5	Design optimization	24/04/2019	8/5/19	Blackboard	Completed
36	5	Design optimization	29/04/2019	9/5/19	Blackboard	Completed
37	5	Design for test	30/04/2019	9/5/19	Blackboard	Completed
38	5	Design for test	03/05/2019 06/05/2019	10/5/19	Blackboard	Completed
39	5	Nontechnical Issues	08/05/2019	13/5/19	Blackboard	Completed
40	5	Nontechnical Issues	10/05/2019 13/05/2019	14/5/19	Blackboard /PPT	Completed

Signature of the Faculty

KOMTAN D. SHINDE

Signature of the HOD

Professor & Head
Dept. of Electronics & Comm. Engg
PESITM, Shivamogga-577204

Signature of the Principal

PES Institute of Technology and Management

Dept. of Electronics & Communication Engineering

Digital System Design using Verilog - 15EC663

Question Bank

Module 1

1. What is meant by the term fanout?.
2. What are the two sources of power consumption in a digital component?
3. What are the TTL output voltage levels, input threshold voltages and noise margins?
4. What is meant by the terms setup time, hold time and clock-to-output time of a fl ip-flop?.
5. For a decoder with inputs (a2, a1, a0), write the Boolean equation for the output corresponding to the code word 100.
6. Identify two approaches to functional verification.
7. What information is specified for each port in a Verilog module?
8. If verification fails during some stage of a design methodology, what action is taken?
9. Develop a Verilog model for a 4-to-1 multiplexer.
10. How does a priority encoder solve the problem of multiple inputs being 1 at the same time?
11. Develop a Verilog model for a 7-segment decoder.
12. Design an encoder for use in a domestic burglar alarm that has sensors for each of eight zones. Each sensor signal is 1 when an intrusion is detected in that zone, and 0 otherwise. The encoder has three bits of output, encoding the zone as follows: Zone 1: 000 Zone 2: 001 Zone 3: 010 Zone 4: 011 Zone 5: 100 Zone 6: 101 Zone 7: 110 Zone 8: 111

Module 2

1. What are the three states of a tristate driver?
2. How do memory components with tristate data outputs simplify construction of large memories?
3. What is the difference between RAM and ROM?
4. What is the difference between static and dynamic RAM?
5. What benefit does a multiport memory have over a single-port memory with multiplexed address and data connections?
6. How does a FIFO facilitate communication of data between clock domains?
7. How can we work out what will happen if we perform concurrent writes to a given location in a synchronous dual-port memory?
8. Using a Hamming code, how many check bits are required for single error correction and double-error detection for 4-bit data words?
9. What corrective action can we take when a parity error is detected?
10. Compute the 12-bit ECC word corresponding to the 8-bit data word 01100001.

Module 3

1. What is photolithography in IC manufacture?
2. How do IC area and defect density on a wafer affect IC cost?
3. What do the terms *ASIC* and *ASSP* stand for?
4. How does a programmable logic device differ from a fixed-function component?
5. What is a fuse map?
6. Use the following components to design a 4-digit decimal counter with a 7-segment LED display: two 74LS390 dual decade counters, four 74LS47 BCD to 7-segment decoders, four 7-segment displays, plus any additional gates required.
7. Derive an expression for the short -circuit trans conductance Gm of the MOS cascade amplifier.
8. If an FPGA uses volatile SRAM cells to store configuration information, how is the configuration information stored and supplied to the FPGA?
9. For a 2.5V low-voltage differential signaling (LVDS) output, the nominal VOL and VOH voltages are 1.075V and 1.425V, respectively. What differential voltage swing is seen at the receiver?
10. Design a priority encoder that has 16 inputs, I[0:15]; a four-bit encoded output, Z[3:0]; and a valid output that is 1 when any input is 1. Input I[0] has the highest priority, and I[15] the lowest priority. The design is to be implemented in a GAL22V10 component.
11. Use the following components to design a 4-digit decimal counter with a 7-segment LED display: two 74LS390 dual decade counters, four 74LS47 BCD to 7-segment decoders, four 7-segment displays, plus any additional gates required.

Module 4

1. What is a sensor? What is an actuator?
2. Why would a digital system require a digital-to-analog converter?
3. How many comparators are required in a flash ADC with a resolution of 8 bits?
4. What is the difference between a solenoid and a relay?
5. What is the purpose of an input register in an I/O controller? What is the purpose of an output register?
6. Write a Verilog statement to model a tri-state driver for an output net d_out. The driver is controlled by a net d_en, and when enabled, drives the value of an input d_in onto the output net.
7. In a multiplexed bus system, why might it be desirable to subdivide the multiplexers and distribute them around the chip?
8. Show how a 64-bit data word can be transmitted serially between two parts of a system. Assume that the transmitter and the receiver are both within the same clock domain, and that the signal start is set to 1 on a clock cycle in which data is ready to be transmitted.
9. Design an interface to connect an embedded Gumnut core to a remote temperature sensor. The temperature sensor is an Analog Devices AD7414 with an I2C connection and an alert output that can be connected to a warning indicator.

Module 5

1. What is meant by the term architecture exploration?
2. What is the distinction between logical partitions and physical partitions of a system?
3. What are the benefits of reusing an IP block to implement a component?
4. Briefly describe the purpose of floor planning, placement, and routing.
5. Why should clock gating not be implemented in RTL model code? How is it better implemented?
6. Describe the difference between code coverage and functional coverage. Which is more important for ensuring correctness of a design?
7. How does IDDQ testing detect transistor stuck-on faults?
8. What purposes do LFSRs and MISRs have in signature-based BIST?
9. Identify some of the main stages in a product's life cycle.
10. Identify a means of improving system performance that we might consider in the architecture exploration stage. What trade-offs arise from improving performance?
11. Synthesize and implement the Sobel accelerator design targeting a Xilinx XC3S200-5 Spartan-3 FPGA with a clock frequency of 100MHz (that is, a clock period of 10ns).
12. Design the control section to sequence computation of the derivative image.

Mr. Kunjan D. Shinde

Mr. Vishwanath Muddi

Asst. Prof. Dept. of E&CE, PESITM.

HOD, ECE

Professor & Head
Dept. of Electronics & Comn Engg
PESITM, Shivamogga-577204

CBCS SCHEME

USN | 4 | P | M | 1 | E | C | 0 | 7 | 6 | | 15EC663

Sixth Semester B.E. Degree Examination, June/July 2019
Digital System Design using Virology

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Define the terms setup time, hold time and clock to output time of a flip-flop and what are the constraints imposed by these parameter on the circuit operations. **(05 Marks)**

b. Develop veriology module for 7 segment decoder. Include an additional input 'blank' that overrides the BCD input and causes all segments not to be lit. **(06 Marks)**

c. Explain functional verification and formal verification for a verilog module **(05 Marks)**

OR

2 a. What are the effects of capacitive loading and propagation delay on signal transitions between logic levels? **(08 Marks)**

b. Develop verilog module for 4 : 1 MUX. **(04 Marks)**

c. Explain general view of digital system with data path control section. **(04 Marks)**

Module-2

3 a. Design a 64k ×8 bit composite memory using four 16k × 8 bit components and also explain how memory components with tristate data outputs simplify the construction of larger memories. **(08 Marks)**

b. Explain asynchronous static RAM with timing diagrams. **(08 Marks)**

OR

4 a. Write a note on multiport memories. **(08 Marks)**

b. Explain error detection and correction with one example. **(08 Marks)**

Module-3

5 a. Explain different types of PCB design. **(05 Marks)**

b. Explain implementation fabrics for digital system based on integrated circuit. **(07 Marks)**

c. What are EMI and cross talk? **(04 Marks)**

OR

6 a. Briefly explain programmable array logic. **(08 Marks)**

b. Explain signal integrity issue in PCB design and also explain measures to reduce these issues. **(08 Marks)**

Module-4

7 a. Explain the serial transmission of 64 bit data within clock domain with timing diagram. **(08 Marks)**

b. Explain the following serial interface standards for connecting I/O devices.
i) RS232 ii) Fire wire. **(08 Marks)**

OR

8 a. Explain any 4 analog sensors. **(08 Marks)**

b. Explain the concept of multiplexed buses **(08 Marks)**

Module-5

9 a. Explain logical partitioning and physical partitioning of a transport monitoring system. **(08 Marks)**

b. Explain fault model and fault simulation. **(08 Marks)**

OR

10 a. Explain 4 bit LFSR and CFSR for generating pseudorandom test vectors. **(08 Marks)**

b. Explain briefly area, power and timing optimization in digital circuits. **(08 Marks)**

* * * * *

15EC663

Visvesvaraya Technological University, Belagavi

MODEL QUESTION PAPER

6th Semester, B.E (CBCS) – Open Elective

Course: 15EC663 – DIGITAL SYSTEM DESIGN USING VERILOG

Time: 3 Hours **Max. Marks: 80**

Note: (i) Answer Five full questions selecting any one full question from each Module.
(ii) Question on a topic of a Module may appear in either its 1st or/and 2nd question.

			Marks
		Module-1	
1	a	What is Digital system? Explain how the Digital circuits are evolved over the times.	5
	b	Define the terms setup time, hold time and clock-to-output time of a flip-flop and what are the constraints imposed by these parameters on the circuit operations?	5
	c	Develop a Verilog model for a 7-segment decoder. Include an additional input, blank, that overrides the BCD input and causes all segments not to be lit.	6
		OR	
2	a	Develop a test bench model for the 3:8 decoder.	6
	b	With an example show the distinction between a Moore and Mealy finite-state machine and also draw the corresponding state transition diagram	10
		Module-2	
3	a	Explain Bidirectional tristate data connections . Design a 64K× 8-bit composite memory using four 16K × 8-bit components using Bidirectional tristate data connections.	8
	b	Develop a Verilog model of the FIFO, which can store up to 256 data items of 16 bits each using 256×16 bit dual port SSRAM for the data storage. The FIFO should provide status outputs *empty* and *full* to indicate the empty and full status of FIFO and FIFO will not be read when it is empty nor be written when it is full and that the write and the read port share a common clock.	8
		OR	
4	a	Design a circuit that computes the function $y=ci \times x^2$, where x is a binary-coded input value and ci is a coefficient stored in a flow-through SSRAM. x, ci and y are all signed fixed-point values with 8 pre binary-point and 12 post-binary-point bits. The index i is also an input to the circuit, encoded as a 12-bit unsigned integer. Values for x and i arrive at the input during the cycle when a control input, start, is 1. The circuit should minimize area by using single multiplier to multiply ci by x and then by x again.	8
	b	What is a common cause of soft errors in DRAMs? Compute the 12-bit ECC word corresponding to the 8-bit data word 01100001.	8
		Module-3	
	a	Explain different types of PCB design. How fast does a signal change propagate along a typical PCB trace?	8

5	b	Explain the concept differential signaling .How does differential signaling improve noise immunity?	8
		OR	
6	a	Explain signal integrity interconnection issue in PCB design.	6
	b	What is the benefit of allowing a PLD in a system to be reprogrammed?	5
	c	What distinguishes a platform FPGA from a simple FPGA?	5
		Module-4	
7	a	Explain Digital-to-Analog Converters using R/2R ladder DAC.	6
	b	Write a Verilog assignment that represents a tri-state bus driver for an 8-bit bus.	6
	c	How does the processor determine where to resume program execution on completion of handling an interrupt?	4
		OR	
8	a	Explain any four serial interface standards.	8
	b	Design and develop the Verilog code for an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in the system.	8
		Module-5	
9	a	Explain the design flow of hardware/software co-design.	10
	b	What aspects of the design flow does a verification plan cover?	6
		OR	
10	a	Explain Built-in self test (BIST) techniques.	8
	b	Explain the terms scan design and boundary scan	8

Sixth Semester B.E. Degree Examination, June/July 2018
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. What are the two sources of power consumption in digital components? Explain. **(04 Marks)**

b. Develop a verilog model for a 4 : 1 multiplexer. **(04 Marks)**

c. Design an encoder for the buglar alarm that has sensors for each of the 8 zones as a priority encoder with zone 1 having highest priority down to zone 8 having lowest priority. **(08 Marks)**

OR

2 a. Explain the simple design methodology followed in IC industry. **(08 Marks)**

b. Develop a datapath to perform complex multiplication of two complex number whose real and imaginary parts are represented as signed fixed point numbers with 4-pre binary points and 12 post-binary points. Real and imaginary parts of the product are represented with 8 pre-binary points and 24 post-binary points. Area is the main constraint. Also write the verilog model of the complex multiplier datapath. **(08 Marks)**

Module-2

3 a. Design a $1m \times 8$ bit composite memory using $512\ K \times 8$ bit memory component. **(04 Marks)**

b. Design a $16K \times 48$ – bit memory using $16K \times 16$ – bit memory component. **(04 Marks)**

c. Explain flowthrough and pipelined SSRAM with the help of timing diagram. **(08 Marks)**

OR

4 a. Determine whether there is an error in the ECC word 000111000100 and if so, correct it. **(06 Marks)**

b. Develop a verilog model of a dual – port $4K \times 16$ bit flow through SSRAM. One port allows data to be written and read, while the other port allows data to be read. **(06 Marks)**

c. Explain dynamic RAM operation. **(04 Marks)**

Module-3

5 a. Write and explain the internal organization of a CPLD. **(08 Marks)**

b. What are the two main design and manufacturing techniques for ASIC's. Explain. **(08 Marks)**

OR

6 a. Write and explain the internal organization of FPGA. **(08 Marks)**

b. Explain differential signaling in detail. **(08 Marks)**

Module-4

7 a. Explain Flash ADC and successive approximation ADC with the help of necessary diagrams. **(08 Marks)**

b. Design an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the I/P value changes. The controller is the only interrupt source in the system. Also develop a verilog model of the I/P controller. **(08 Marks)**

OR

8 a. Explain the following serial interface standards for connecting I/O devices: (08 Marks)
(i) I²C (ii) USB

b. With a neat diagram, explain R-string DAC and R-2R ladder DAC. (08 Marks)

Module-5

9 a. Explain the design flow of hardware/software co-design. (10 Marks)

b. Explain floorplan, placement and routing of ASIC physical design. (06 Marks)

OR

10 a. Explain Built-In Self Test (BIST) techniques. (08 Marks)

b. Explain the terms scan design and boundary scan. (08 Marks)

PESITM
education for the real world

PES Institute of Technology and Management,
NH-206, Sagar Road, Shivamogga-577204
Department of Electronics and Communication Engineering

Internal Assessment 1

Subject & Code : Digital System Design Verilog(15EC663)
Semester : 6th Sem, A & B Division
Course Instructor : KDS VM

Max. Marks : 30
Date : 08/03/19
Timings : 1:30pm to 2:45pm

Sl.No		Questions	CO's	Blooms levels	Marks
		Note: Answer any one full question from each module			
		Module 1			
1	a	With neat diagram explain embedded system hardware and software co-design	CO1	L2	06M
	b	Explain the following real world constraints (i) logic levels (ii) capacitive load and propagation delay (iii) power	CO1	L3	09M
2	a	With a neat diagram, explain digital IC design methodology.	CO2	L2	8M
	b	Design the traffic light control system and write the testbench to Verify the conditions that, when the enable input is 1, the output is the same as the light input, and when the enable input is 0, all light outputs are inactive.**(use one hot codes for lights →100-red, 010-yellow, 001- green).**	CO2	L3	7M
		Module 2			
3	a	Design a Verilog model for a 7-segment decoder. Include an additional input, blank, that overrides the BCD input and causes all segments not to be lit.	CO2	L3	7M
	b	Design a Verilog model of the implement complex multiplier with datapath & control unit.	CO2	L3	8M
4	a	Design a 64K x 8-bit composite memory using four 16K x 8-bit components.	CO1	L3	10M
	b	What is memory & explain the same using symbol for basic memory component	CO2	L2	5M

Course instructor

Reviewer

HOD,ECE

Professor & Head
Dept. of Electronics & Comm. Engg.
PESITM, Shivamogga-577204

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NH-206, Sagar Road, Shivamogga-577204
Department of Electronics and Communication Engineering

Quiz (version A)

Subject & Code : **Digital System Design Using Verilog HDL (15EC663)** Semester : **6th Sem, A & B Division**

Sl. No.	Questions (All are compulsory and carry 1 marks each)	
1	Full form of HDL	1Mark
2	Which of the following is case sensitive (a) Verilog HDL (b) VHDL (c) both a and b (d) none	1Mark
3	Which of the following is not a verilog data type a) X b)0 c) 1 d) A	1Mark
4	A variable 'sum' of 3-bit is defined as a) [0:3] sum b) [3:0] sum c)sum [3:0] d) both a & b	1Mark
5	One hot codes are the codes in which a) only one bit is 1 b) multiple bits are 1 c) both a & b d) none	1Mark
6	In verilog the integer datatypes are defined by using the key word (a) integer (b)real (c) Decimal (d) float	1Mark
7	In moore machines the output depends on a) only state b) input and current state c) only input d) none	1Mark
8	Which of the following is not a keyword (a) module (b) task (c) endtask (d) disp	1Mark
9	Which block has a sensitivity list (a) initial (b) always (c) if-else (d) assign	1Mark
10	Noise margin high (NM_H) =..... Noise margin low (NM_L) =.....	1Mark

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PES Institute of Technology and Management,
NH-206, Sagar Road, Shivamogga-577204
Department of Electronics and Communication Engineering

Quiz (version B)

Subject & Code : **Digital System Design Using Verilog HDL (15EC663)** Semester : **6th Sem, A & B Division**

Sl. No.	Questions (All are compulsory and carry 1 marks each)	
1	In verilog the integer datatypes are defined by using the key word (a) integer (b)real (c) Decimal (d) float	1Mark
2	In moore machines the output depends on a) only state b) input and current state c) only input d) none	1Mark
3	Which of the following is not a keyword (a) module (b) task (c) endtask (d) disp	1Mark
4	Which block has a sensitivity list (a) initial (b) always (c) if-else (d) assign	1Mark
5	Noise margin high (NM_H) =..... Noise margin low (NM_L) =.....	1Mark
6	Full form of HDL	1Mark
7	Which of the following is case sensitive (a) Verilog HDL (b) VHDL (c) both a and b (d) none	1Mark
	Which of the following is not a verilog data type a) X b)0 c) 1 d) A	1Mark
9	A variable 'sum' of 3-bit is defined as a) [0:3] sum b) [3:0] sum c)sum [3:0] d) both a & b	1Mark
10	One hot codes are the codes in which a) only one bit is 1 b) multiple bits are 1 c) both a & b d) none	1Mark

Course instructor

Reviewer

HOD,ECE

Professor & Head
Dept. of Electronics & Comm Engg
PESITM Shivamogga-577204

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Department of Electronics and Communication Engineering

Quiz (version A)

Subject & Code : **Digital System Design Using Verilog HDL (15EC663)** Semester : **6th Sem, A & B Division**

Sl. No.	Questions (All are compulsory and carry 1 marks each)	
1	Full form of HDL	1Mark
2	Which of the following is case sensitive (a) Verilog HDL (b) VHDL (c) both a and b (d) none	1Mark
3	Which of the following is not a verilog data type a) X b)0 c) 1 d) A	1Mark
4	A variable 'sum' of 3-bit is defined as a) [0:3] sum b) [3:0] sum c)sum [3:0] d) both a & b	1Mark
5	One hot codes are the codes in which a) only one bit is 1 b) multiple bits are 1 c) both a & b d) none	1Mark
6	In verilog the integer datatypes are defined by using the key word (a) integer (b)real (c) Decimal (d) float	1Mark
7	In moore machines the output depends on a) only state b) input and current state c) only input d) none	1Mark
8	Which of the following is not a keyword (a) module (b) task (c) endtask (d) disp	1Mark
9	Which block has a sensitivity list (a) initial (b) always (c) if-else (d) assign	1Mark
10	Noise margin high (NM_H) = $V_{oH} - V_{iH}$ Noise margin low (NM_L) = $V_{iL} - V_{oL}$	1Mark

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Internal Assessment 1

Subject & Code : Digital System Design Verilog(15EC663)
Semester : 6th Sem, A & B Division
Course Instructor :

Max. Marks : 30
Date :
Timings :

SL.No		Questions Note: Answer any one full question from each module	COs	Blooms levels	Marks
		Module 1			
1	a	With neat diagram explain embedded system hardware and software co-design	CO1	L2	06M
	b	Explain the following real world constraints (i) logic levels (ii) capacitive load and propagation delay (iii) power	CO1	L3	09M
2	a	With a neat diagram, explain digital IC design methodology.	CO2	L2	8M
	b	Design the traffic light control system and write the testbench to Verify the conditions that, when the enable input is 1, the output is the same as the light input, and when the enable input is 0, all light outputs are inactive.**(use one hot codes for lights →100-red, 010-yellow, 001- green).**	CO2	L3	7M
		Module 2			
3	a	Design a Verilog model for a 7-segment decoder. Include an additional input, blank, that overrides the BCD input and causes all segments not to be lit.	CO2	L3	7M
	b	Design a Verilog model of the implement complex multiplier with datapath & control unit.	CO2	L3	8M
4	a	Design a 64K x 8-bit composite memory using four 16K x 8-bit components.	CO1	L3	10M
	b	What is memory & explain the same using symbol for basic memory component	CO2	L2	5M

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Scheme of Evaluation

Digital System Design using Verilog HDL, 15EC663, 6th Semester

Q. No.	Solution - IA I. 02/03/2019.	Marks

Q1. a. Hardware Software Co-design.

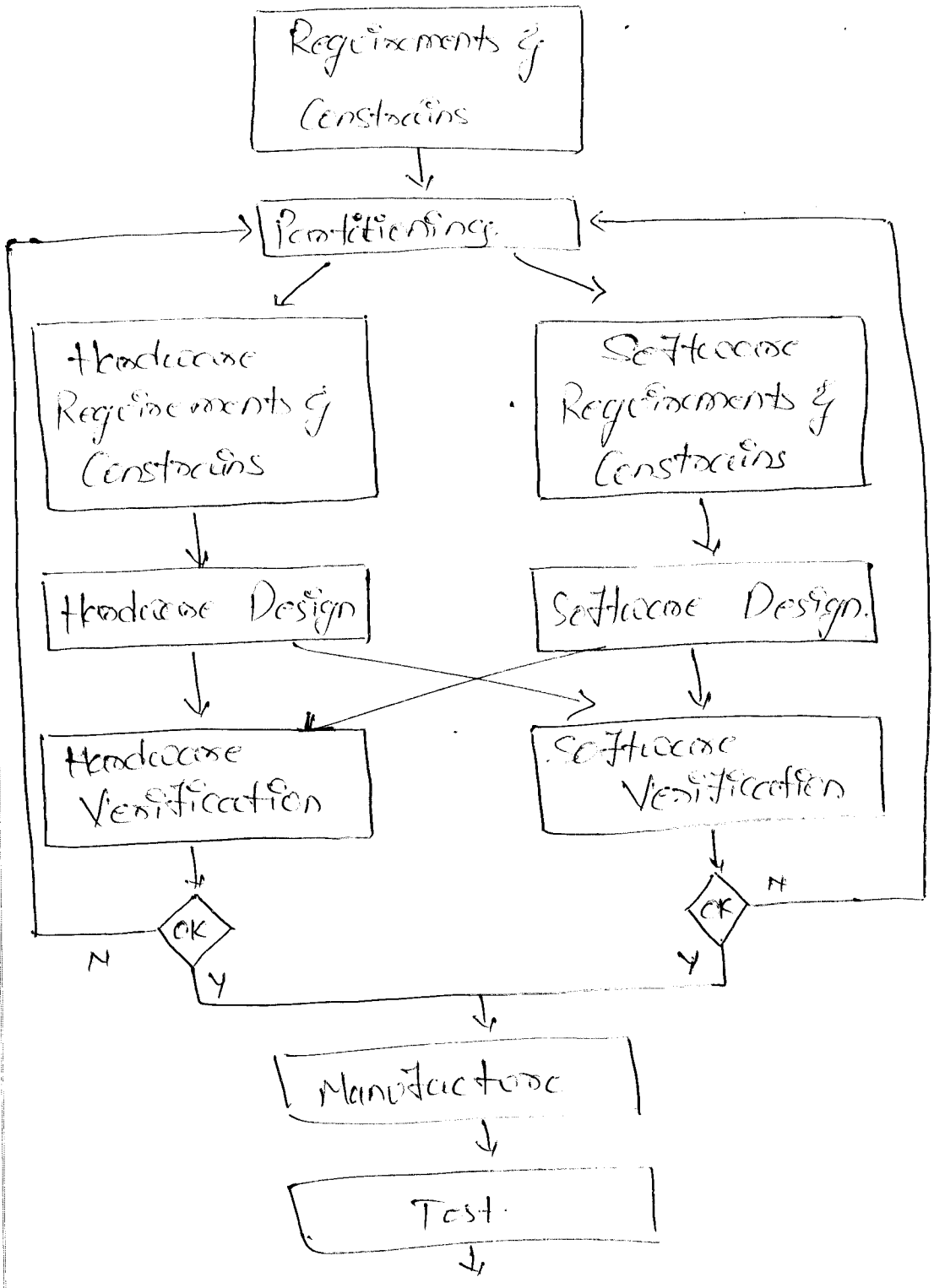
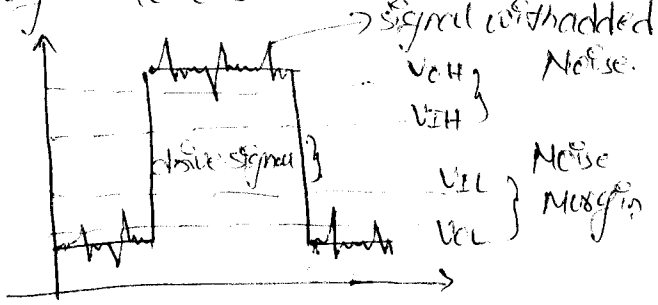
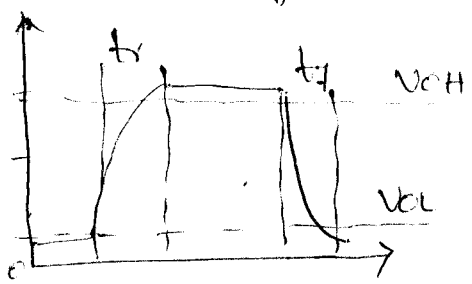
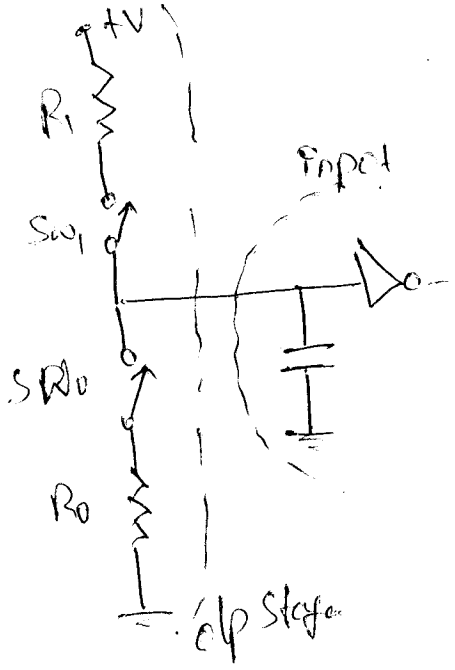
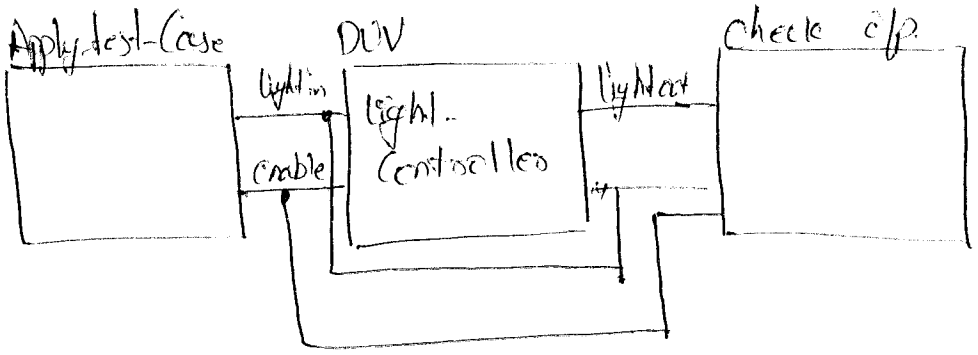


Diagram & Explanation

03+
03
06M

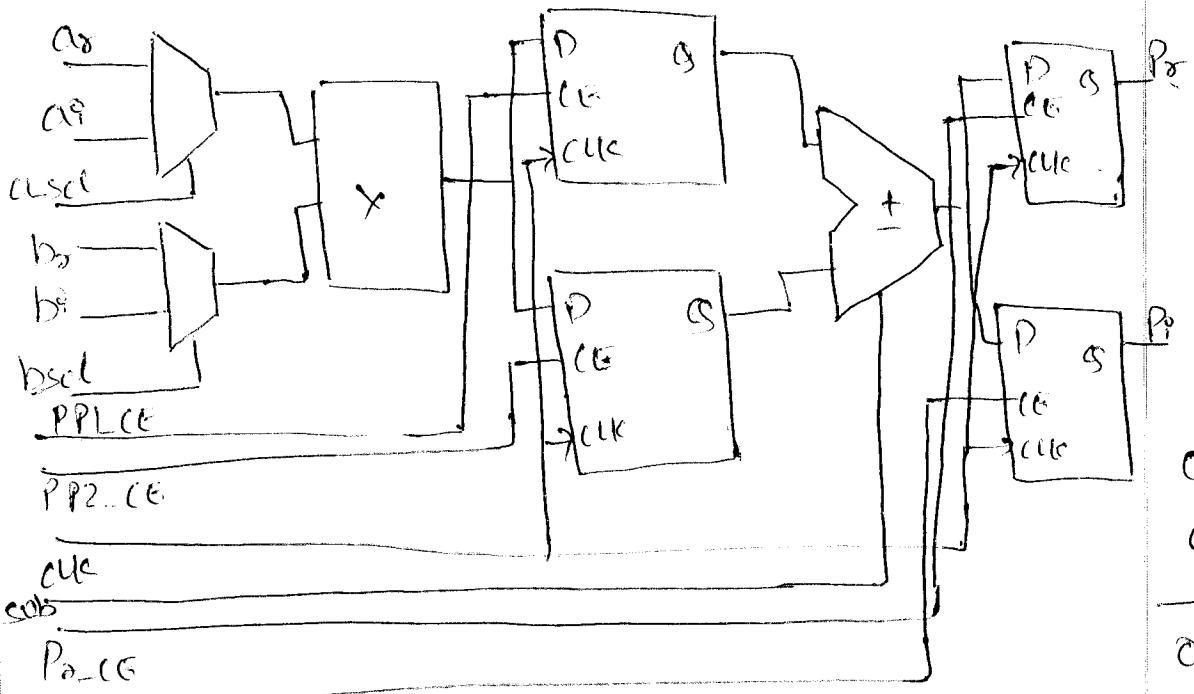
Q. No.	Solution	Marks
Q1.b.	Logic levels  - Delay Power - Static Power - Dynamic Power Capacitive load & propagation delay  	03x3 09M
Q2.b.	 Design of the Light Controller Testbench to verify the conditions	02 05 07M

Q. No.	Solution	Marks
33.b	Complex multiplier with datapath & control unit	

$a = a_R + j a_I$; $b = b_R + j b_I$

$P = a \cdot b = a_R b_R + j(a_R b_I + a_I b_R) - a_I b_I$

$P = a_R b_R - a_I b_I + j(a_R b_I + a_I b_R)$

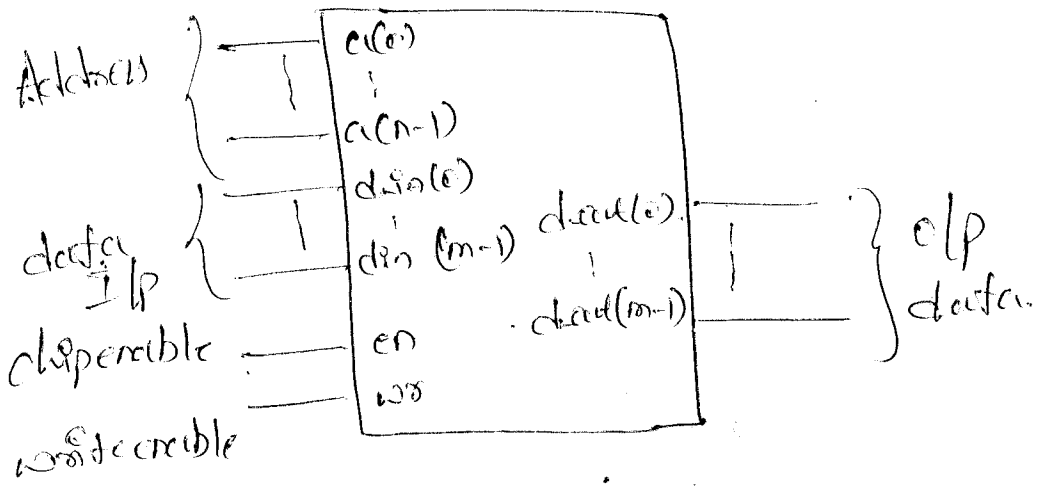


CLA
CM

08M

- Design & Verilog HDL coding with control sequence.

Step	a_sel	b_sel	pp1_ce	pp2_ce	sub	P_R_ce	P_I_ce
1	0	0	1	0	0	0	0
2	1	1	0	1	-	0	0
3	0	1	1	0	1	1	0
4	1	0	0	1	0	0	0
5	-	-	0	0	0	0	1

Q. No.	Solution	Marks
5(4.b.	Definition of memory: Conceptually an array of storage elements/registers or locations - each location distinct address - No of locations - power of 2. - Address range 0 to $2^n - 1$ - n-bit address - m-bit data stored per location. - Memory capacity 2^n bytes (locations) x m bits - Conceptually: Symbol of basic memory component  - width - m-bits - length/size - 2^n locations	02 03 05M
5(1.a.	1. Hardware description language 2. Verilog HDL 3. A 4. both a & b. 5. only 1 bit is '1' 6. integer 7. current state 8. disp 9. always 10. $V_{CH} - V_{IH}$, $V_{IL} - V_{CL}$ (high, low)	
Version A		

Subject In-charge

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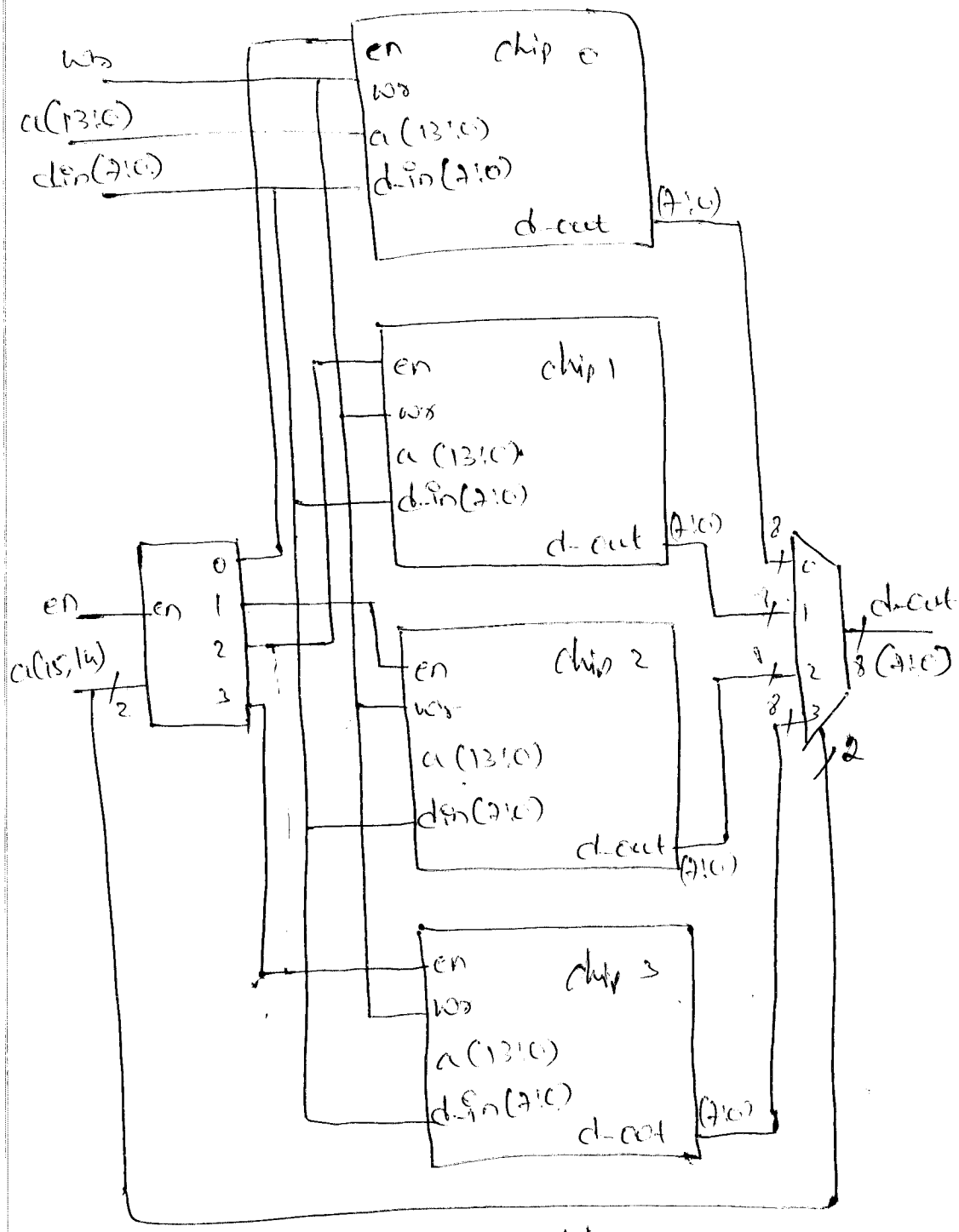
Q. No.	Solution	Marks
Q4.a.	64K x 8bit Composite memory using 16K x 8bit.	



a15	a14	Y_3	Y_2	Y_1	Y_0	chip
0	0	0	0	0	1	0
0	1	0	0	1	0	1
1	0	0	1	0	0	2
1	1	1	0	0	0	3

Design, working & explanation

5+
3+
2
10M

PES Institute of Technology and Management

Dept. of Electronics & Communication Engineering

Digital System Design using Verilog (15EC663)

Internal Assessment - 1

Poor Performance (Slow learners) students list 6th A

Sl. No.	Name	USN	
1.	MEGHARAJACHARI	4PM15EC045	12/30
2.	AKSHAY KUMAR M	4PM16EC005	9/30
3.	ANUSHA NS	008	15/30
4.	DUNDUBI R	021	15/30
5.	KAVYA GC	033	6/30
6.	LIKITHA R	037	13/30
7.	CHETANA BC	4PM16EC403	14/30
8.			
9.			
10.			

Action Taken:

1. Students with poor performance were asked to solve the IA & P1 & Submit the same.
2. ~~Tutorial~~ Question bank with some typical questions for upcoming syllabus was provided. ~~Early~~ ~~MCQ~~

15/2/19

Subject In Charge

15/2/19

HOD ECE

Professor & Head
Dept. of Electronics & Comm. Engg
PES Inst. of Technology

PES Institute of Technology and Management

Dept. of Electronics & Communication Engineering,

Digital System Design Using Verilog HDL (15EC663)			
Internal Assessments 1 Marks			
Sl. No	USN	Name	IA Test-1
1	4PM14EC048	Pallavi	26.0
2	4PM15EC006	Angel Priya M	24.0
3	4PM15EC013	Arpitha S V	29.0
4	4PM15EC029	Ganesh Prasad D M	19.0
5	4PM15EC041	Madhu S Bhat	18.0
6	4PM15EC045	Megharajachari B	12.0
7	4PM15EC051	Neha P	20.0
8	4PM16EC002	Aishwarya Channayya Hiremath	25.0
9	4PM16EC004	Aishwarya Shashidhar Kolgi	28.0
10	4PM16EC005	Akshay Kumar M	9.0
11	4PM16EC007	Anusha B G	29.0
12	4PM16EC008	Anusha N S	15.0
13	4PM16EC010	Arpitha L	26.0
14	4PM16EC012	Asha G M	28.0
15	4PM16EC015	Chaithra K C	22.0
16	4PM16EC018	Deepa Hondad	25.0
17	4PM16EC020	Dixitha Chandrakanth Shet	27.0
18	4PM16EC021	Dundubi R	15.0
19	4PM16EC022	Ganavi C G	29.0

20	4PM16EC023	Ganesha N	21.0
21	4PM16EC026	Halaswamy S R	24.0
22	4PM16EC029	Harshitha M K	21.0
23	4PM16EC030	Harshitha S	26.0
24	4PM16EC033	Kavya G C	6.0
25	4PM16EC037	Likitha R	13.0
26	4PM16EC038	M Monisha	Absent
27	4PM16EC039	Madhushrees S Shet	22.0
28	4PM16EC040	Manjanaik S B	22.0
29	4PM16EC042	Neha D G	24.0
30	4PM16EC043	Nehashri S	24.0
31	4PM16EC044	Nida Khanum	22.0
32	4PM16EC045	Nihar K K	26.0
33	4PM16EC050	Pallavi M P	27.0
34	4PM16EC403	Chetana B C	14.0
35	4PM16EC412	Maruthi T L	19.0
36	4PM17EC401	Abhishek Gowda N R	16.0
37	4PM17EC403	Bharathkumar H S	26.0
38	4PM17EC405	Kavya B	18.0
39	4PM17EC408	Lokesh C	25.0
40	4PM17EC412	Pramodkumar S Vagannanavar	21.0

Subject Incharge

Mr. Kunjan D. Shinde
Asst. Professor, Dept. Of E&CE,
PESITM, Shivamogga.

Hod, ECE

Dr. Chandrappa D N

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Department of Electronics and Communication Engineering

Internal Assessment II

Subject & Code : Digital System Design Verilog(15EC663)
Semester : 6th Sem, A & B Division
Course Instructor : Mr. Kunjan D Shindhe & Mr. Vishwanath Muddi

Max. Marks : 30
Date : 13 /04/2019
Timings : 1:30 to 2:45pm

Sl.No		Questions Note: Answer any one full question from each module	CO's	Blooms levels	Marks
		Module 1			
1	a	Design a circuit that computes the function $y = ci *x^2$, where x is a binary-coded input value and c_i is a coefficient stored in a flow-through SSRAM. x, c_i and y are all signed fixed-point values with 8 pre binary-point and 12 post-binary-point bits. The index i is also an input to the circuit, encoded as a 12-bit unsigned integer. Values for x and i arrive at the input during the cycle when a control input, start, is 1. The circuit should minimize area by using a single multiplier to multiply c_i by x and then by x again.	CO1	L2	8M
	b	With neat timing diagram explain the working of asynchronous RAM	CO1	L3	7M
2	a	Develop a Verilog model of a dual-port, 4K x 16-bit flow-through SSRAM. One port allows data to be written and read, while the other port only allows data to be read.	CO2	L2	7M
	b	Determine whether there is an error in the ECC word 000111000100, and if so, correct it.	CO2	L3	8M
		Module 2			
3	a	With neat diagram explain steps involved in IC manufacturing steps.	CO2	L3	7M
	b	With neat diagram explain internal organization of CPLD.	CO2	L3	8M
	a	With neat diagram explain internal organization of FPGA.	CO1	L3	9M
	b	Write short note on packaging and circuit boards	CO2	L2	6M

Course instructor

Reviewer

HOD,ECE

Professor & Head
Dept. of Electronics & Comm Engg
PESITM, Shivamogga-577204

PES Institute of Technology and Management,
NH-206, Sagar Road, Shivamogga-577204
Department of Electronics and Communication Engineering

Quiz (version A)

Subject & Code : **Digital System Design Using Verilog HDL (15EC663)** Semester : **6th Sem, A & B Division**

Sl. No.	Questions (All are compulsory and carry 1 marks each)	
1	Full form of FIFO	1Mark
2	Kilo in memory indicates _____ number of locations i) 2^{10} ii)2^{30} iii)2^{40} iv) none	1Mark
3	SRAM stands for	1Mark
4	Expansion of EEPROM	1Mark
5	DRAM uses _____ to store the bits i) capacitor ii) inductor iii) flip-flop iv) resistor	1Mark
6	PCB stands for_____	1Mark
7	Look up tables are present in i) FPGA ii)CPLD iii) ROM iv) PLD	1Mark
8	Which of the following can be reconfigured i) combinational ROM ii)FPGA iii)ASICs iv) none	1Mark
9	Silicon is widely used to manufacture ICs because it is i) Abundant ii) rare material iii) easily oxidized	1Mark
10	Formula used in differential signalling is _____	1Mark

PES Institute of Technology and Management,
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Department of Electronics and Communication Engineering

Quiz (version B)

Subject & Code : **Digital System Design Using Verilog HDL (15EC663)** Semester : **6th Sem, A & B Division**

Sl. No.	Questions (All are compulsory and carry 1 marks each)	
1	PCB stands for_____	1Mark
2	Look up tables are present in i) FPGA ii)CPLD iii) ROM iv) PLD	1Mark
3	Which of the following can be reconfigured i) combinational ROM ii)FPGA iii)ASICs iv) none	1Mark
4	Silicon is widely used to manufacture ICs because it is i) Abundant ii) rare material iii) easily oxidized	1Mark
5	Formula used in differential signalling is _____	1Mark
6	Full form of FIFO	1Mark
7	Kilo in memory indicates _____ number of locations i) 2^{10} ii)2^{30} iii)2^{40} iv) none	1Mark
8	SRAM stands for	1Mark
9	Expansion of EEPROM	1Mark
10	DRAM uses _____ to store the bits i) capacitor ii) inductor iii) flip-flop iv) resistor	1Mark

Course instructor

Reviewer

HOD,ECE

Professor & Head
Dept. of Electronics & Comm Engg
PESITM, Shivamogga-577204

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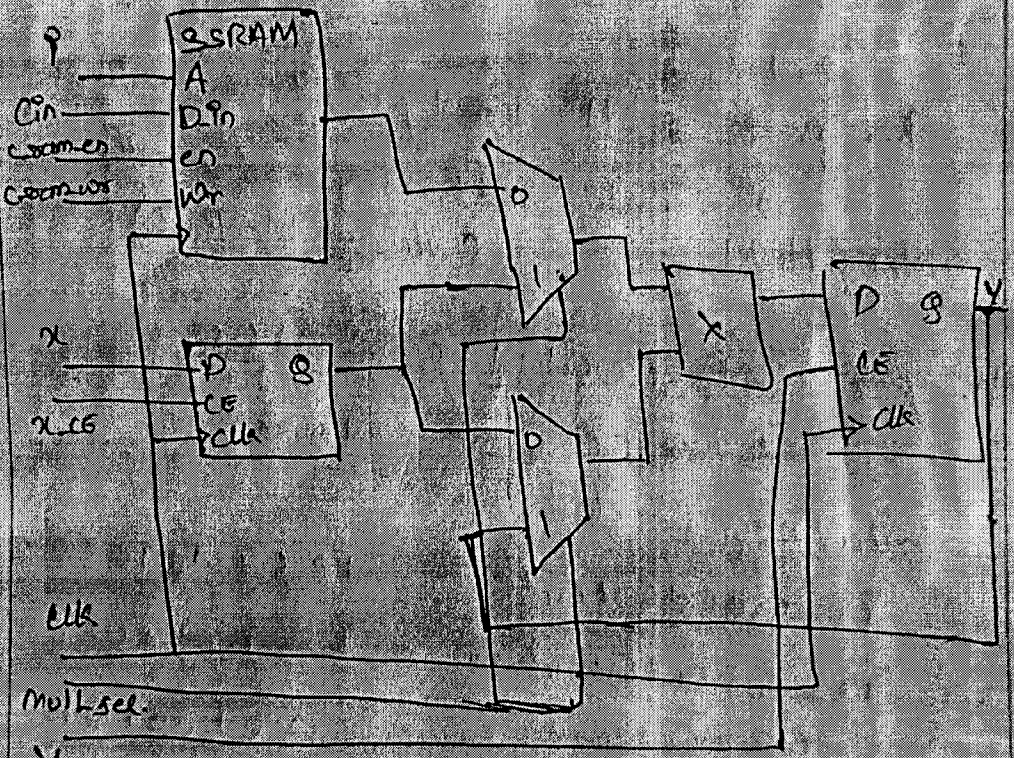
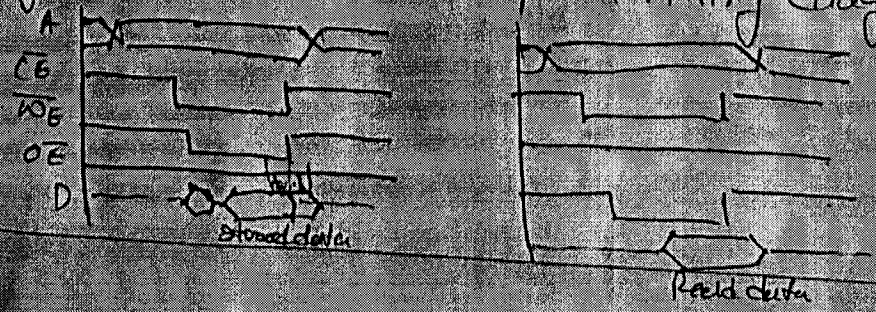
Department of Electronics & Communication Engineering

Internal Assessment-

Scheme & Solutions

Subject Name & Code: DSDV (15EC663) Sem: VI

Faculty Name: ANJAN D. SHINDE Max Marks: 30

Question No.	Solution	Marks Allotted
1.a.		03
	Timing diagram with state transition diagram, Explanation with pin & past binary value	02 03 08M
1.b.	Asynchronous SSRAM Concept + Timing diagram 	03 04 07M

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Question No.	Solution	Marks Allotted

8a.	Verilog model for 4K×16 bit SSRAM Dual Port.
	* reg [15:0] data-RAM [0:4095]; // creates memory reg
	two ports port1: Ready write operation
	port2: Read operation only.
	always block1 (always block 2)
		07M

8b.	ECC word: 0001 1100 0100 check bits from ECC word: 1000 calculating check bits $c_1 = c_3 \oplus c_5 \oplus c_7 \oplus c_9 \oplus c_{11} = 1 \oplus 0 \oplus 0 \oplus 0 \oplus 0 = 1$ $c_2 = c_3 \oplus c_6 \oplus c_7 \oplus c_{10} \oplus c_{11} = 1 \oplus 0 \oplus 0 \oplus 0 \oplus 0 = 0$ $c_4 = c_5 \oplus c_6 \oplus c_7 \oplus c_{12} = 0 \oplus 0 \oplus 0 \oplus 0 = 0$ $c_8 = c_9 \oplus c_{10} \oplus c_{11} \oplus c_{12} = 0 \oplus 0 \oplus 0 \oplus 1 = 1$ check bits obtained = 1101 Syndrom = 1101 ⊕ 1000 = 0101 ∴ Error in 5th bit; Corrected ECC: 0001101010004	04 04 08M

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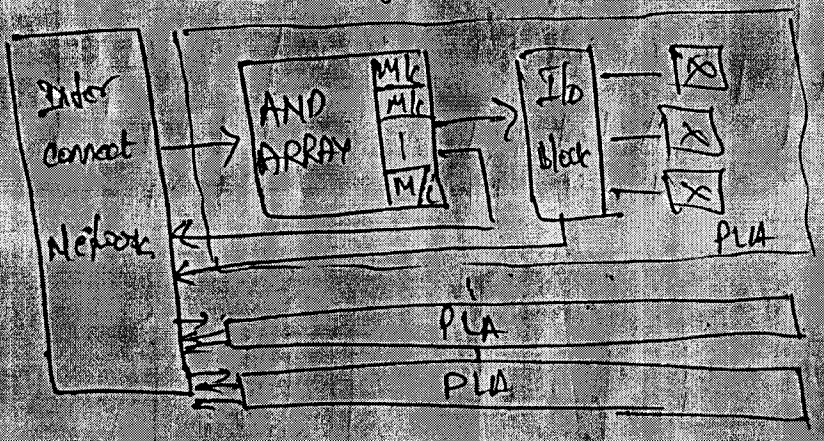
Question No.	Solution	Marks Allotted
Q3.a.	Steps involved in IC Manufacturing. - Wafer - Photolithography - Ionization - Etching - Metallization, expln in detail.	07M
Q3.b.	CPLD Internal organization 	04
	Explanation - Prog AND ARRAY, Macro of PLA.	04
		08M
Q4.a.	IC package, - PCB, through hole, insertion types SIP, DIP, Surface-mount PCB BGA PGA - Multichip modules,	06M

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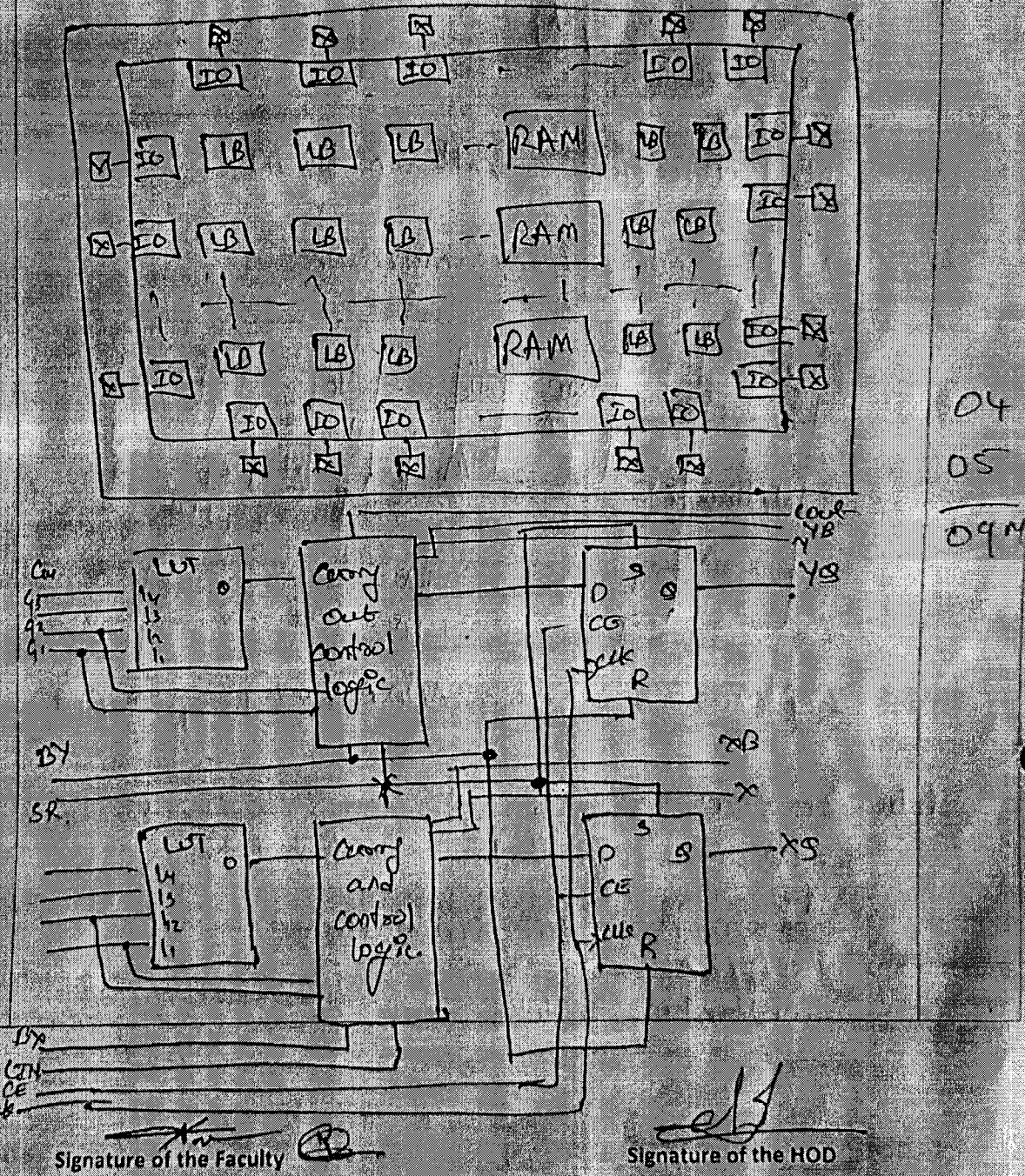
Question No.	Solution	Marks Allotted
4.a	Internal organization of an FPGA. 	04 05 09M

Signature of the Faculty

RANJAN D. SHINDE

VISHWANATH MUDDI

Signature of the HOD

PES Institute of Technology and Management

Dept. of Electronics & Communication Engineering

Digital System Design using Verilog (15EC663)

Internal Assessment - 2

Poor Performance (Slow learners) students list 6th A

Sl. No.	Name	USN	
1.	Pallavi	4PM14EC048	13/30
2.	Ganeshprasad DM	4PM15EC029	12/30
3.	Madhu S Bhat	4PM15EC041	14/30
4.	Neha P	4PM15EC051	14/30
5.	Akshay Kumar S	4PM16EC005	14/30
6.	Dundubi	4PM16EC021	14/30
7.	Chethan BC	4PM16EC403	07/30
8.			
9.			
10.			

Action Taken:

1. Selection of IA 2 for continious poor performance students.
2. Tutorial Extra class was conducted for the poor performance Students on 04/4/19, 11/4/19

16/4/19

Subject In Charge

16/4/19

HOD ECE

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PES Institute of Technology and Management

Dept. of Electronics & Communication Engineering,

Digital System Design Using Verilog HDL (15EC663)			
Internal Assessments 2 Marks			
Sl. No	**USN**	**Name**	**IA Test-2**
1	4PM14EC048	Pallavi	13.0
2	4PM15EC006	Angel Priya M	Absent
3	4PM15EC013	Arpitha S V	29.0
4	4PM15EC029	Ganesh Prasad D M	12.0
5	4PM15EC041	Madhu S Bhat	14.0
6	4PM15EC045	Megharajachari B	19.0
7	4PM15EC051	Neha P	14.0
8	4PM16EC002	Aishwarya Channayya Hiremath	28.0
9	4PM16EC004	Aishwarya Shashidhar Kolgi	Absent
10	4PM16EC005	Akshay Kumar M	14.0
11	4PM16EC007	Anusha B G	29.0
12	4PM16EC008	Anusha N S	24.0
13	4PM16EC010	Arpitha L	27.0
14	4PM16EC012	Asha G M	28.0
15	4PM16EC015	Chaithra K C	22.0
16	4PM16EC018	Deepa Hondad	27.0
17	4PM16EC020	Dixitha Chandrakanth Shet	18.0
18	4PM16EC021	Dundubi R	14.0
19	4PM16EC022	Ganavi C G	28.0

20	4PM16EC023	Ganesha N	28.0
21	4PM16EC026	Halaswamy S R	20.0
22	4PM16EC029	Harshitha M K	Absent
23	4PM16EC030	Harshitha S	29.0
24	4PM16EC033	Kavya G C	23.0
25	4PM16EC037	Likitha R	20.0
26	4PM16EC038	M Monisha	16.0
27	4PM16EC039	Madhushrees S Shet	Absent
28	4PM16EC040	Manjanaik S B	Absent
29	4PM16EC042	Neha D G	22.0
30	4PM16EC043	Nehashri S	21.0
31	4PM16EC044	Nida Khanum	Absent
32	4PM16EC045	Nihar K K	20.0
33	4PM16EC050	Pallavi M P	25.0
34	4PM16EC403	Chetana B C	7.0
35	4PM16EC412	Maruthi T L	23.0
36	4PM17EC401	Abhishek Gowda N R	25.0
37	4PM17EC403	Bharathkumar H S	23.0
38	4PM17EC405	Kavya B	Absent
39	4PM17EC408	Lokesh C	24.0
40	4PM17EC412	Pramodkumar S Vagannanavar	Absent

Subject Incharge

Mr. Kunjan D. Shinde
Asst. Professor, Dept. Of E&CE,
PESITM, Shivamogga.

Hod, ECE

Dr. Chandrappa D N

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PES Institute of Technology and Management,
NH-206, Sagar Road, Shivamogga-577204
Department of Electronics and Communication Engineering

Internal Assessment III

Subject & Code : Digital System Design Verilog(15EC663)
Semester : 6th Sem, A & B Division
Course Instructor : Mr. Kunjan D Shindhe & Mr.Vishwanath Muddi

Max. Marks : 30
Date :15 /05/201
Timings : 1:30 to 2:45pm

Sl.No		Questions	CO's	Blooms levels	Marks
		Note: Answer any one full question from each module			
		Part-A			
1	a	Explain serial interface standards	CO5	L3	7M
	b	Explain the operation of multiplexed bus & Tristate bus.	CO5	L3	8M
2	a	Write a short note on I/O software	CO5	L2	7M
	b	Show how a 64-bit data word can be transmitted serially between two parts of a system. Assume that the transmitter and the receiver are both within the same clock domain, and that the signal start is set to 1 on a clock cycle in which data is ready to be transmitted.	CO2	L3	8M
		Part-B			
	a	Write a short note on 1) area optimization 2) BIST	CO4	L2	7M
	b	Explain architectural exploration and partitioning steps with an example.	CO2	L2	8M
4	a	Explain functional design and functional verification.	CO4	L2	7M
	b	With neat diagram explain prototypical design flow including hardware/software codesign.	CO2	L2	8M

Course instructor

Reviewer

HOD,ECE

Professor & Head
Dept. of Electronics & Comm. Engg
PESITM, Shivamogga-577204

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Department of Electronics and Communication Engineering

Quiz (version A)

Subject & Code : **Digital System Design Using Verilog HDL (15EC663)** Semester : **6th Sem, A & B Division**

Sl. No.	Questions (All are compulsory and carry 1 marks each)	
1	Full form of EDA_____	1Mark
2	In hardware/software co-verification _____is used to test instruction sets.	1Mark
3	Serial communication uses _____number of buses to transmit data	1Mark
4	Transducers are used to interact with _____	1Mark
5	Expand DAC_____	1Mark
6	In physical designing arranging different blocks in a orderly manner is called as_____planning	1Mark
7	What is the other name for interval timer?	1Mark
8	Each segment of an LCD consists of_____ material	1Mark
9	The simplest I/O synchronization mechanism is called as_____	1Mark
10	Multiplexer has_____ouputs. a)1 b)2 c)3 d)n	1Mark

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Department of Electronics and Communication Engineering

Quiz (version B)

Subject & Code : **Digital System Design Using Verilog HDL (15EC663)** Semester : **6th Sem, A & B Division**

Sl. No.	Questions (All are compulsory and carry 1 marks each)	
1	In physical designing arranging different blocks in a orderly manner is called as_____planning	1Mark
2	What is the other name for interval timer?	1Mark
3	Each segment of an LCD consists of_____ material	1Mark
4	The simplest I/O synchronization mechanism is called as_____	1Mark
5	Multiplexer has_____ouputs. a)1 b)2 c)3 d)n	1Mark
6	Full form of EDA_____	1Mark
7	In hardware/software co-verification _____is used to test instruction sets.	1Mark
8	Serial communication uses _____number of buses to transmit data	1Mark
9	Transducers are used to interact with _____	1Mark
10	Expand DAC_____	1Mark

Course instructor

Reviewer

HOD,ECE

Professor & Head
Dept. of Electronics & Comm. Engg
PESITM, Shivamogga-577204

PES Institute of Technology and Management,
NH-206, Sagar Road, Shivamogga-577204
Department of Electronics and Communication Engineering

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Internal Assessment III

Subject & Code : Digital System Design Verilog(15EC663)
Semester : 6th Sem, A & B Division
Course Instructor : Mr. Kunjan D Shindhe & Mr.Vishwanath Muddi

Max. Marks : 30
Date : /05/201
Timings :

Sl.No		Questions	CO's	Blooms levels	Marks
		Note: Answer any one full question from each module			
		Part-A			
1	a	Explain serial interface standards	CO5	L3	7M
	b	Explain the operation of multiplexed bus & Tristate bus.	CO5	L3	8M
2	a	Write a short note on I/O software	CO5	L2	7M
	b	Show how a 64-bit data word can be transmitted serially between two parts of a system. Assume that the transmitter and the receiver are both within the same clock domain. and that the signal start is set to 1 on a clock cycle in which data is ready to be transmitted.	CO2	L3	8M
		Part-B			
3	a	Write a short note on 1) area optimization 2) BIST	CO4	L2	7M
	b	Explain architectural exploration and partitioning steps with an example.	CO2	L2	8M
4	a	Explain functional design and functional verification.	CO4	L2	7M
	b	With neat diagram explain prototypical design flow including hardware/software codesign.	CO2	L2	8M

PES Institute of Technology and Management,
NH-206, Sagar Road, Shivamogga-577204
Department of Electronics and Communication Engineering

Quiz (version A)

Subject & Code : **Digital System Design Using Verilog HDL (15EC663)** Semester : **6th Sem, A & B Division**

Sl. No.	Questions (All are compulsory and carry 1 marks each)	
1	Full form of EDA Electronic Design Automation	1 Mark
2	In hardware/software co-verification Enumerator is used to test instruction sets.	1 Mark
3	Serial communication uses 1 number of buses to transmit data	1 Mark
4	Transducers are used to interact with Physical world / real world.	1 Mark
5	Expand DAC Digital to Analog converter.	1 Mark
6	In physical designing arranging different blocks in a orderly manner is called as floor planning	1 Mark
7	What is the other name for interval timer?	1 Mark
8	Each segment of an LCD consists of Liquid crystal. material	1 Mark
9	The simplest I/O synchronization mechanism is called as Polling.	1 Mark
10	Multiplexer has 1 ouputs. a)1 b)2 c)3 d)n	1 Mark

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Department of Electronics and Communication Engineering

Quiz (version B)

Subject & Code : **Digital System Design Using Verilog HDL (15EC663)** Semester : **6th Sem, A & B Division**

Sl. No.	Questions (All are compulsory and carry 1 marks each)	
1	In physical designing arranging different blocks in a orderly manner is called as_____planning	1 Mark
2	What is the other name for interval timer?	1 Mark
3	Each segment of an LCD consists of _____ material	1 Mark
4	The simplest I/O synchronization mechanism is called as_____	1 Mark
5	Multiplexer has_____ouputs. a)1 b)2 c)3 d)n	1 Mark
6	Full form of EDA_____	1 Mark
7	In hardware/software co-verification is used to test instruction sets.	1 Mark
8	Serial communication uses _____ number of buses to transmit data	1 Mark
9	Transducers are used to interact with _____	1 Mark
10	Expand DAC _____	1 Mark

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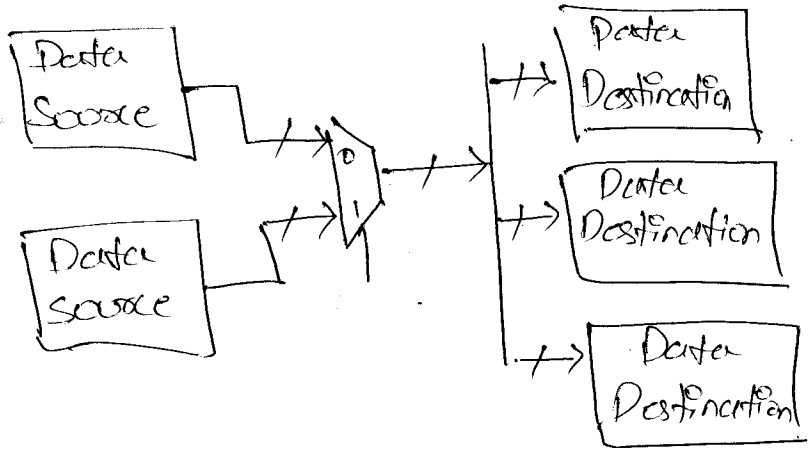
Scheme of Evaluation

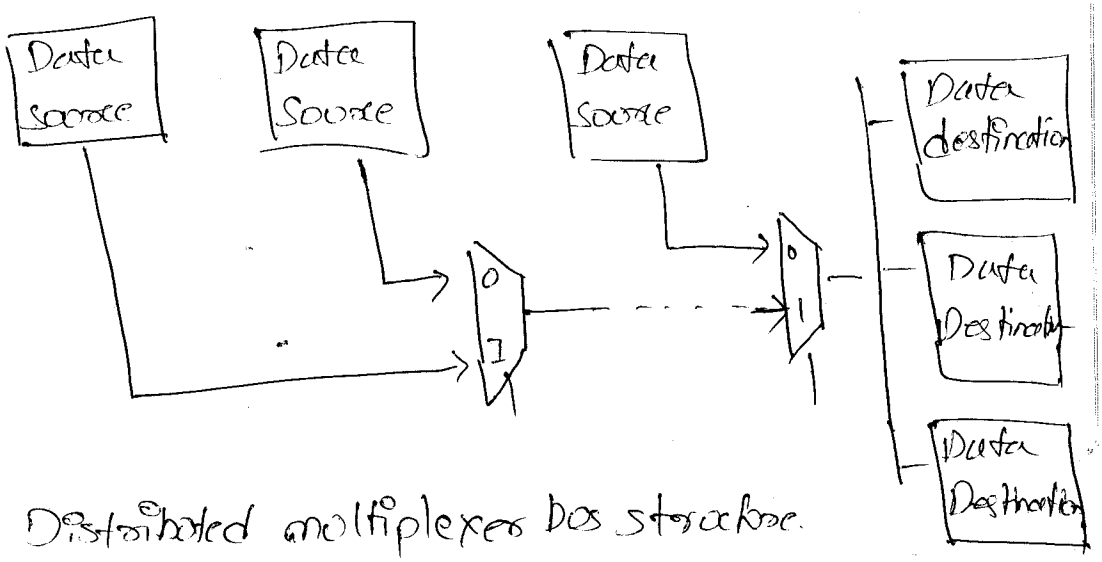
Digital System Design using Verilog HDL, 15EC663, 6th Semester

Q. No.	Solution IA SP - 3	Marks
Q1.a.	Serial Interface standards	
	- RS232 – NRZ encoding - LSB 1st MSB LAST Eg. Barcode.	1
	- I^2C – NRZ coded - Tx^n b/w chips – 10kbit/sec to 3.4 Mbit/sec	2
	- USB – Modified NRZ – 1.5, 12, 480 Mbits/sec. - Pair of wires	2
	- Fire wire – IEEE standard 1394, High speed (400 Mbits/s) upto 3.2 Gbit/sec - two pair differential signalling pairs.	2
		7M
Q1.b.	Multiplexed bus:	



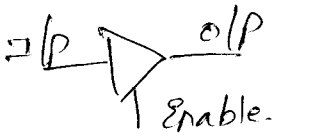
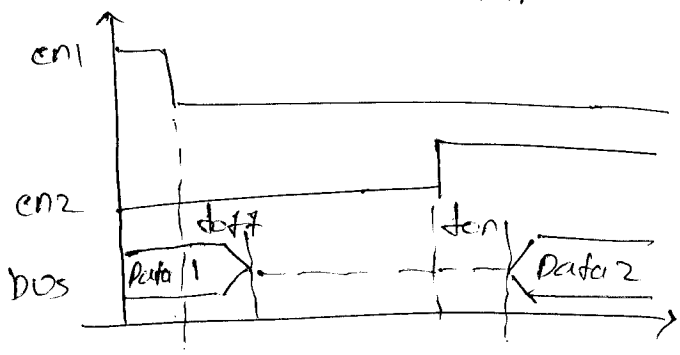
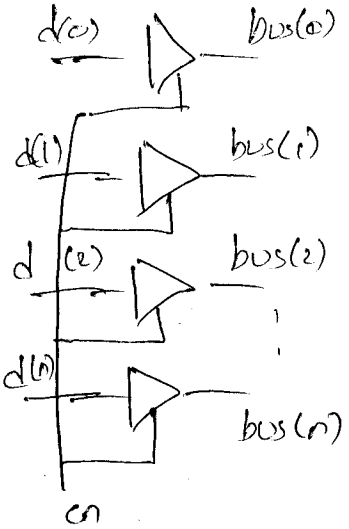
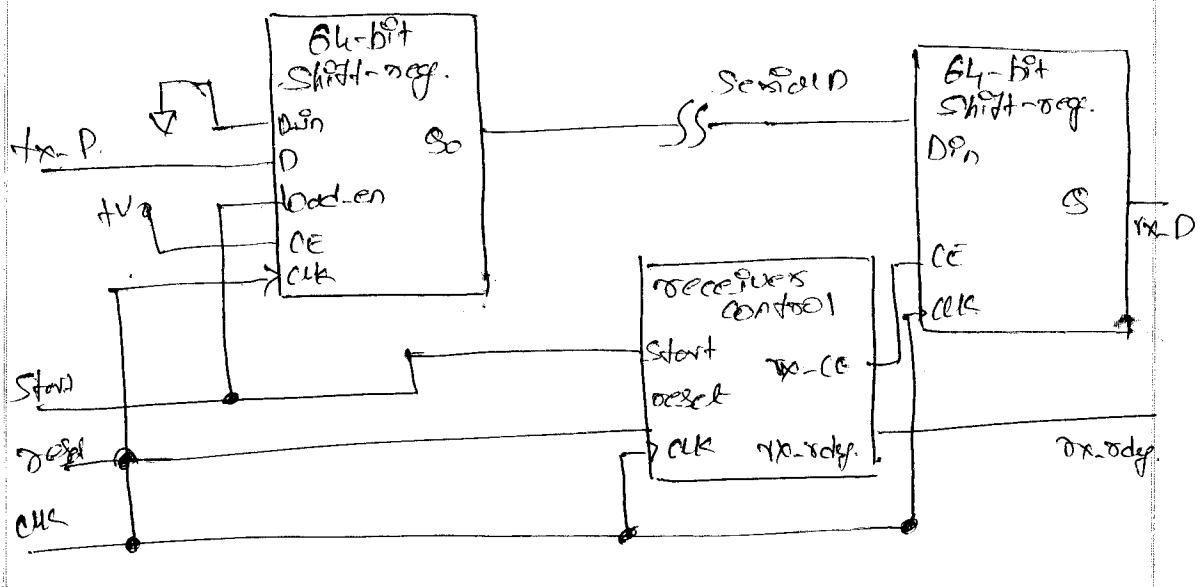
2.5 M

Bus using multiplexer to select among data sources.



2.5M

Distributed multiplexer bus structure.

Q. No.	Solution	Marks
	Tristate bus    Tristate disable & enable timing.	03 08M
Q2.a.	Short note on I/O Software. - Polling – Continious monitoring - Processor busy with only one task to scan I/ps. - Interrupt. - ISR - Interrupt Service routine - IH - Interrupt Handler - Priorities - Masking / nested interrupts.	03M 04M
		07M
Q2.b.	64-bit data word transmitted Serially. 	

Q4.a. Functional Design.

- Architecture spec decomposed into physical comp.
- Behavioural Model
- Intellectual property - reusable components.
- Core Generation - EDA tool.
- Memories ALU, Bus interface, DSP, FSM.

3.5M

Functional Verification

- Simulation based Verification of functionality
- What function to verify.
- What part to verify.
- How to verify.
- Code Coverage.
- Function Coverage.
- directed testing.

3.5M

7M.

Q4.b. Design flow of H/w S/w codesign. process typical - with neat diagram & explanation. 08M

Unit 7 A Version

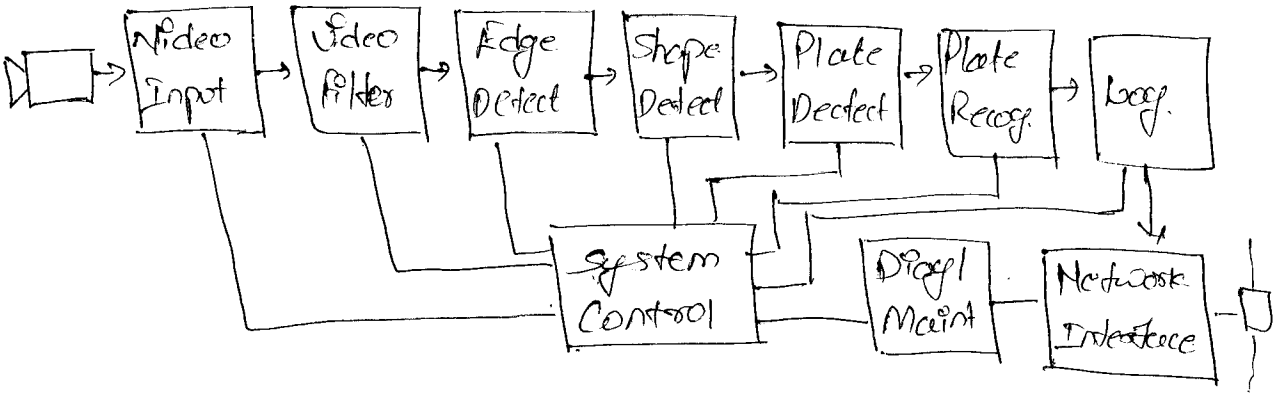
1) Electronic Design Automation
2) Emulator.
3) one
4) Physical world/
5) Digital to Analog Converter.
6) Floor planning.
7) ~~Floor planning~~. Real time clock.
8) Liquid crystal.
9) Polling.
10) one.

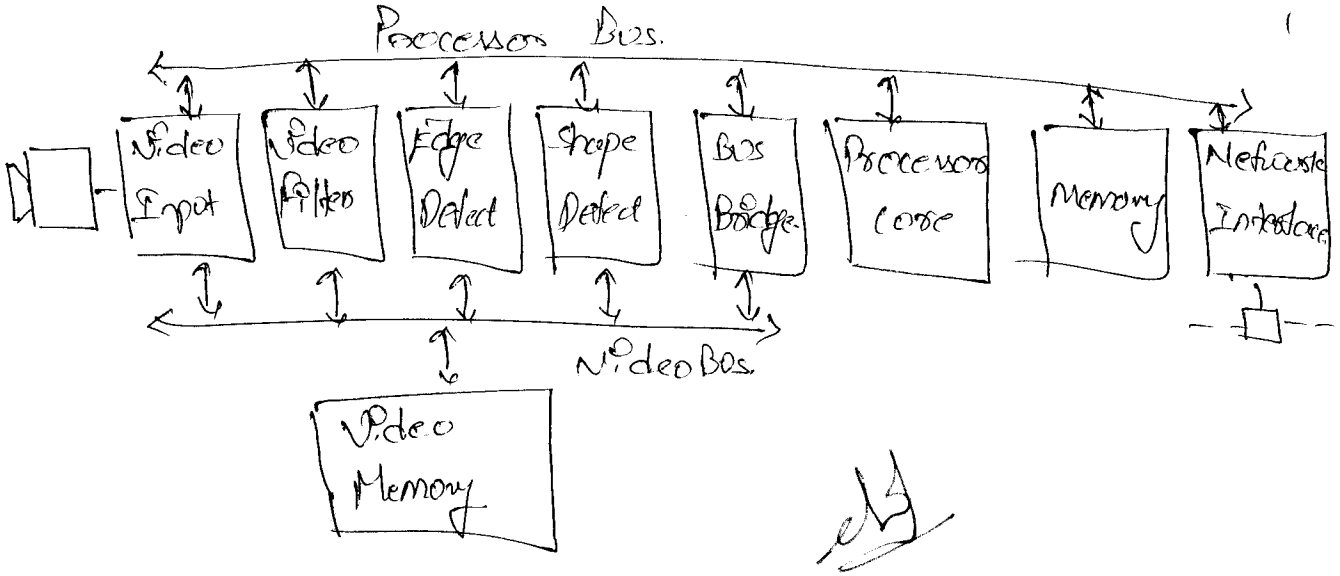
Q2.b - Short Note.

- Area optimization - chip area, lead to package cost, 03M
  Floorplanning, partitioning.
- BIST - Built In Self Test.
  - Pseudo Random test pattern generators.
  - Linear feedback shift register (LFSR)
  - Complet " " " (CFSR) 04M

07M

Q3.b. Architectural exploration & partitioning steps.





PES Institute of Technology and Management

Dept. of Electronics & Communication Engineering

Digital System Design using Verilog (15EC663)

Internal Assessment - 3

Poor Performance (Slow learners) students list 6th A

Sl. No.	Name	USN
1.	Lokesh C	4PM17EC408 9/30
2.		
3.		
4.		
5.		
6.		
7.		
8.		
9.		
10.		

Action Taken:

1. Student had IA1-25, IA2-24, so the student might not have performed Good.

17/5/19.

Subject In Charge

17/5/19

HOD ECE

Professor & Head
Dept. of Electronics & Comm Engg
PESITM, Shivamogga-577204

PES Institute of Technology and Management

Dept. of Electronics & Communication Engineering,

Digital System Design Using Verilog HDL (15EC663)			
Internal Assessments 3 Marks			
Sl. No	**USN**	**Name**	**IA Test-3**
1	4PM14EC048	Pallavi	29.0
2	4PM15EC006	Angel Priya M	28.0
3	4PM15EC013	Arpitha S V	Absent
4	4PM15EC029	Ganesh Prasad D M	28.0
5	4PM15EC041	Madhu S Bhat	27.0
6	4PM15EC045	Megharajachari B	23.0
7	4PM15EC051	Neha P	18.0
8	4PM16EC002	Aishwarya Channayya Hiremath	28.0
9	4PM16EC004	Aishwarya Shashidhar Kolgi	28.0
10	4PM16EC005	Akshay Kumar M	26.0
11	4PM16EC007	Anusha B G	Absent
12	4PM16EC008	Anusha N S	24.0
13	4PM16EC010	Arpitha L	Absent
14	4PM16EC012	Asha G M	Absent
15	4PM16EC015	Chaithra K C	29.0
16	4PM16EC018	Deepa Hondad	Absent
17	4PM16EC020	Dixitha Chandrakanth Shet	Absent
18	4PM16EC021	Dundubi R	25.0
19	4PM16EC022	Ganavi C G	Absent

20	4PM16EC023	Ganesha N	Absent
21	4PM16EC026	Halaswamy S R	Absent
22	4PM16EC029	Harshitha M K	29.0
23	4PM16EC030	Harshitha S	Absent
24	4PM16EC033	Kavya G C	20.0
25	4PM16EC037	Likitha R	28.0
26	4PM16EC038	M Monisha	27.0
27	4PM16EC039	Madhushrees S Shet	28.0
28	4PM16EC040	Manjanaik S B	26.0
29	4PM16EC042	Neha D G	26.0
30	4PM16EC043	Nehashri S	Absent
31	4PM16EC044	Nida Khanum	28.0
32	4PM16EC045	Nihar K K	Absent
33	4PM16EC050	Pallavi M P	Absent
34	4PM16EC403	Chetana B C	28.0
35	4PM16EC412	Maruthi T L	25.0
36	4PM17EC401	Abhishek Gowda N R	28.0
37	4PM17EC403	Bharathkumar H S	Absent
38	4PM17EC405	Kavya B	27.0
39	4PM17EC408	Lokesh C	9.0
40	4PM17EC412	Pramodkumar S Vagannanavar	26.0

Subject Incharge

Mr. Kunjan D. Shinde
Asst. Professor. Dept. Of E&CE.
PESITM. Shivamogga.

Hod, ECE

Dr. Chandrappa D N

Digital System Design using Verilog HDL (15EC663)

Internal Assessments Marks

Sl. No	USN	NAME	IA Test-1	IA Test-2	IA Test-3	Quiz	Avg.	Sign.
1	4PM14EC048	PALLAVI	26.0	13.0	29.0	8	18	Pallavi
2	4PM15EC006	ANGEL PRIYA M	24.0	Absent	28.0	5	16	
3	4PM15EC013	ARPITHA S V	29.0	29.0	Absent	9	19	
4	4PM15EC029	GANESH PRASAD D M	19.0	12.0	28.0	7	16	
5	4PM15EC041	MADHU S BHAT	18.0	14.0	27.0	8	16	Madhu
6	4PM15EC045	MEGHARAJACHAR I B	12.0	19.0	23.0	10	16	
7	4PM15EC051	NEHA P	20.0	14.0	18.0	8	14	
8	4PM16EC002	AISHWARYA CHANNAYYA HIREMATH	25.0	28.0	28.0	8	18	
9	4PM16EC004	AISHWARYA SHASHIDHAR KOLGI	28.0	Absent	28.0	6	17	Aishwarya
10	4PM16EC005	AKSHAY KUMAR M	9.0	14.0	26.0	9	15	
11	4PM16EC007	ANUSHA B G	29.0	29.0	Absent	10	20	
12	4PM16EC008	ANUSHA N S	15.0	24.0	24.0	7	16	
13	4PM16EC010	ARPITHA L	26.0	27.0	Absent	10	19	
14	4PM16EC012	ASHA G M	28.0	28.0	Absent	10	20	Asha.G.M
15	4PM16EC015	CHAITHRA K C	22.0	22.0	29.0	8	17	
16	4PM16EC018	DEEPA HONDAD	25.0	27.0	Absent	10	18	Deepa
17	4PM16EC020	DIXITHA CHANDRAKANTH SHET	27.0	18.0	Absent	9	16	
18	4PM16EC021	DUNDUBI R	15.0	14.0	25.0	8	14	Dundubi R
19	4PM16EC022	GANAVI C G	29.0	28.0	Absent	10	20	Ganavi.C